1 SERT Component Update Requirements

1.1 Introduction

In the quickly evolving world of computer servers, software updates are needed to enable support for new hardware and software platforms, to address software bugs, or to enhance usability. However, to accurately compare SEEM results, consistency in elements which affect the measurement, is required. Additionally, when SEEM is implemented, it is imperative that changes which affect result comparability are not introduced for the duration of the program. To accommodate these requirements, the following test plans have been developed to maintain comparability of measurement results while allowing updates.

1.2 SEEM Component Versions and Allowed Updates

1.2.1 SEEM v1.x and *SEEM_IDLE*v1.x Component Versions

For SEEM v1.x and *SEEM_IDLE*v1.x, only the below component versions shall be used.

SERT: Version 2.0.1 (initial version) and later versions 2.x.x which comply with Sub Clause 1.3.2.

PTDaemon: Version 1.8.1 (initial version) or later versions that comply with Sub Clause 1.3.3.

SERT Client Configuration XML: CPU architecture, OS, and JVM version sets listed in *Annex A*, or which comply with Sub Clause 1.3.4.

SERT Run and Reporting Rules: Only Version 2.0.1 (20170929), which is available at https://www.spec.org/sert2/SERT-runrules-20170929.pdf.

Power Analysers: Power analyser models listed in *Annex B*, or power analyser which complies with all the requirements of all Sub Clauses within 1.3.5.

Temperature Sensors: Temperature sensor models listed in *Annex B*, or any temperature sensor which complies with all the requirements of Sub Clause 1.3.6.

1.3 Requirements for New Software and Hardware Compliance

1.3.1 Introduction

In order to ensure accuracy and comparability of results for a specific version of SEEM, the Sub Clauses of this section define requirements which ensure result comparability between all testing software and hardware components.

1.3.2 SERT

Updated minor versions of SERT shall be tested with the following test plan and meet the stated requirements:

1) Select two servers which are currently available for sale from *Annex A*, or that have been shown to be compliant with SEEM. Select two OSes which are developed by different companies, and two CPU architectures developed by different companies.

2) For each configuration, run a baseline compliant SERT run using the initial version of SERT (specified in Sub Clause 9.2.1).

3) For each configuration, run a compliant SERT run using the new version of SERT.

4) Per configuration, the overall SERT efficiency score shall not differ more than 3%, between the original and new version of SERT. Additionally, per configuration, the 100% performance score of each CPU and Memory SERT worklet shall not differ by more than 10%.

1.3.3 PTDaemon

Updated versions of PTDaemon shall be tested with the following test plan and meet the stated requirements:

1) Select at least two different controller system OSes, two different servers which are still available for sale, two temperature sensors, and two power analysers. The selected power analysers must be manufactured by different companies, and it is preferred, but not required, that the temperature sensors are of different models and manufacturers. All selected power analyser and temperature sensor must be included in *Annex B*.

2) Select and configure a server to run SERT. Select and configure a controller system with one of the selected OSes. Connect one power analyser and temperature sensor to the SUT.

3) Install the initial version of PTDaemon (as specified in Sub Clause 1.2.1)

4) Run the SERT test

5) Install and configure the new version of PTDaemon

6) Run the SERT test

7) Repeat steps 1 through 6 one more using the second server, power analyser, and temperature sensor. Also, reconfigure the controller system with a second OS.

8) For each hardware configuration, per SERT worklet, the sum of the average-watts measured with the initial version and new version of PTDaemon shall differ by less than 5%, and the average temperature difference per worklet shall be less than 3°C.

1.3.4 SERT Client Configuration XML

1.3.4.1 *Introduction*

The SERT Client Configuration XML is a file within SERT which consists of a list of sets of CPUs, Operating Systems, and JVMs which can be used with the SERT tool. The HTML version of this list is available at https://www.spec.org/sert2/SERT-JVM_Options-2.0.html, and the XML version for use during testing, is available at https://www.spec.org/sert2/client-configurations-2.0.xml. *Annex A* includes a list of sets of CPUs, OSes, and JVMs which are approved for use with SEEM.

This sub clause includes the requirements and test plans which must be completed successfully for a new CPU, OS, and JVM set to be compliant with SEEM. To create a new client configuration, a set of JVM optimization flags which all comply with the requirements of Sub Clause 1.3.4.2 must be selected. Also, the applicable test plan from Sub Clause 1.3.4.3 must be successfully completed. Finally, software support for a new set is required within the SERT tool. SPEC has a process for this support to be added, which is described in Section 4 of the SERT Run Rules, which is available at: https://www.spec.org/sert2/SERT-runrules-20170929.pdf. This SPEC adoption process may include additional requirements to those described in these Sub Clauses.

1.3.4.2 *JVM Flag Requirements*

Compliant configurations must only use JVM flags which meet the following requirements:

1) Described in publicly available documentation from the JVM vendor

2) Supported for use in production environments

3) Does not disable Reliability, Availability, or Serviceability (RAS) features that are enabled by default in the JVM

4) Does not cause applications to behave in ways contrary to the Java Virtual Machine specification. For example, this requirement would preclude options that relax the level of precision required by mathematical operations.

5) Does not enable optimizations that target the specific code sequences executed by the SERT suite. Optimizations must be expected to improve performance or power consumption of a wider class of applications than the SERT suite.

1.3.4.3 *SERT Invalid Messages*

1.3.4.3.1 Introduction

SERT includes a comprehensive error checking system which produces *Invalid* and *Warning* messages for many reasons. When completing compliance testing, the tester is expected to encounter some *Invalid* messages, such as those stating the configuration being tested is not included in the Client Configuration XML. This section defines two groups of *Invalid* messages, and some sections of the test plan state the situations where encountering these messages is allowed. Note, these two groups do not include all possible SERT *Invalid* messages.

1.3.4.3.2 Group A Invalid Messages

The following is the list of all the *Invalid* message in Group A. The symbols <> denotes a field that SERT fills in dynamically, such as a version number or a field name.

1) *This result was obtained with a development build <> and may not be used for compliant results*

2) *This result was obtained with a trial version of SERT <> and may not be used for compliant results*

3) *The specified client configuration <> could not be found in the client configurations file*

4) *The client configuration <> does not contain a client specification for <>*

5) *The client count for <> in client configuration <> does not match the definition from the client configurations file*

6) *The option set for <> in client configuration <> does not match the definition from the client configurations file*

7) *No signature found for <>*

8) *The <> file has been modified*

9) *The signature for <> is invalid*

10) *One or more TestEnvironment entries (including <>) uses a default value (beginning with "_")*

11) *The node Quantity (<>) is invalid. It must be an integer value.*

12) *The <> date is formatted incorrectly. The correct format is YYYY-MM (actual date was <>)*

13) *No power analyzer was used for this run*

14) *The power analyzer <> is not an accepted device*

15) *No temperature sensor was used for this run*

16) *The temperature sensor <> is not an accepted device*

1.3.4.3.3 Group B Invalid Messages

The following is the list of all the *Invalid* message in Group B. The symbols <> denote a field that SERT fills in dynamically, such as a numeric test value.

1) *Transactions per second was <> of target (threshold is at least <>)*

2) *Transactions per second was <> of target (threshold is at most <>)*

3) *The coefficient of variation among hosts was <>, which is greater than the threshold of <>*

1.3.4.4 *CPU and Software Compliance Test Plans*

1.3.4.4.1 Introduction

Once software support for a new CPU architecture, OS, and JVM has been added to SERT through the SPEC process, the applicable test plan must be successfully completed for the configuration to be compliant with SEEM. On a given CPU architecture, when a major OS or JVM has been shown to be compliant, all future minor updates to that OS or JVM are also considered compliant without retesting.

Unless otherwise noted, only single runs of each of the test points is required. Where identical testing is required in multiple sections of a test plan, the test only needs to be run once. It is allowed to use normalized results when demonstrating compliance. For all test cases and all selected configurations, the JVM, OS and CPUs of the architecture being tested for compliance, must be used and all required outcomes must be satisfied.

For the CPU Compliance Test Plans, the tester can choose to obtain compliance for the entire CPU architecture, or only a set of CPU models or socket types within a CPU architecture, referred to as a CPU architecture portion. For instance, if a new CPU architecture supports 1, 2, and 4 socket configurations, the tester could choose to only obtain compliance for 1 and 2 socket configurations. Later, the tester could obtain compliance for 4 socket configurations with additional testing. If a tester is only obtaining support for a CPU architecture portion, this must be specified in the testing report, and the scope of the test plan will be reduced to the portion being tested to obtain compliance.

While executing all test plans in Sub Clause 1.3.4.4, it is expected and allowed to encounter SERT *Warning* messages as well as SERT *Group A Invalid* messages, as defined in Sub Clause 1.3.4.3. No SERT *Invalid* messages are allowed during testing performed for use in SEEM government regulations or programs.

All configs must use balanced memory configurations, with memory evenly distributed between processors and at least one DIMM populated per memory channel. If no platform of the CPU

architecture, or architecture portion, supports a balanced memory configuration, then imbalanced memory configs may be used.

1.3.4.4.2 Software Minor Update Compliance Test Plan

Minor updates to compliant major versions of OSes or JVMs are already considered compliant. This test plan is intended for situations where changes to JVM flags or other settings are desired for a new minor update to a compliant OS or JVM.

Compliance for a new OS or JVM version can only be obtained with this test plan if one of the following is applicable:

1) Adding support for a new minor JVM or OS version when the major JVM or OS version is already supported on the desired OS and CPU architecture

2) Adding support for a new OS variant which is already supported for the same CPU architecture. A common example is a Linux distribution which has many similar components to a compliant Linux distribution. New major versions of Operating Systems cannot gain compliance with this test plan. This test plan only applies when there are no changes to the JVM version or flags, no software updates to SERT, and the only required changes are to the Client Configuration XML file.

Test Plan:

1) Run a series of 5 consecutive SERT runs using all elements of the new configuration

2) At most, 1 of the 5 runs can include one or more SERT *Group B Invalid* messages, as defined in Sub Clause 1.3.4.3.3

3) The coefficient of variation (CV) for each SERT worklet must be less than 10%

1.3.4.4.3 Software Compliance Test Plan

Compliance for OS or JVM versions which use a compliant CPU architecture, can be shown to be compliant by successfully completing the following test plan. If compliance for a new OS, JVM, and CPU architecture is desired, the correct CPU Compliance Test Plan must be completed instead of this test plan. In some situations, the reduced test plan of Sub Clause 1.3.4.4.2 is applicable and can be used instead of this test plan.

Test Plan:

1) CPU Socket Testing

a) Run SERT on two socket counts, one being the largest socket count which is supported on the CPU architecture. If the CPU architecture only supports one socket count, only test with this socket count. For this testing, all server CPU sockets shall be populated with CPUs.

Required outcomes:

For every test point, a SERT result with no *Group B Invalid Messages* (Sub Clause 1.3.4.3.3) must be completed

2) Memory Size Testing

a) For a selected configuration, test 2 supported memory sizes. If no platform of this CPU architecture supports more than 1 memory size, only complete test *b)*. The balanced memory requirement stated in Sub Clause 1.3.4.4.1 must be followed for all selected memory configurations.

b) A selected size equal to, or larger than, 25% of the max memory size supported. The selected size must be different from that selected in *c)*.

c) The second selected size shall be the larger of 8GB and the Minimum Balanced Memory Size for the selected server, as calculated in *Equation 11*.

Required outcome:
For every test point, a SERT result with no *Group B Invalid Messages* (Sub Clause 1.3.4.3.3) must be completed

3) Disk Quantity Testing

Run SERT on 2 different quantities of disks. If no platform of this CPU architecture supports 2 or more disks, run with the most different quantities supported. It is recommended to run with the maximum number of disks supported to ensure functionality across all disk controllers and connections.

Required outcome:
For every test point, a SERT result with no *Group B Invalid Messages* (Sub Clause 1.3.4.3.3) must be completed

4) Storage Technology Testing

Run SERT with 2 different storage devices using different technologies, for example HDDs and SSDs. If no platform of this CPU architecture supports 2 different types of storage technologies, run with only 1 type of disk. If the only storage devices supported are HDDs, test with two different rotational speeds, and only one speed if two rotation speeds are not supported.

Required outcome:
For every test point, a SERT result with no *Group B Invalid Messages* (Sub Clause 1.3.4.3.3) must be completed

5) Validity and Variance Testing

Run a series of 5 consecutive SERT runs on a selected configuration

Required outcomes:
a) At most, 1 of the 5 runs can include one or more SERT *Group B Invalid* messages, as defined in Sub Clause 1.3.4.3.3

b) The coefficient of variation (CV) for each SERT worklet must be less than 10%

1.3.4.4.4 CPU Model Compliance Test Plan

Compliance for one or more new CPU models can only be obtained with this test plan if the following is applicable:

Adding support for one or more new CPU models within a compliant CPU architecture, which use the same CPU socket type as previously shown to be compliant. New socket counts may be shown to be compliant using this test plan. Only compliant JVM and OS versions for this CPU architecture may be used.

When testing new CPU models for compliance, the tester must identify which socket counts are being tested for compliance. This selection will affect the scope of the test plan and determine which CPUs and socket counts receive an entry in the Client Configuration XML file.

Test plan:

1) Select a configuration which meets all of the following requirements

a) CPU socket count is the largest of the new CPU models being tested

b) The CPU core count is the largest supported of the new CPU models being tested

c) The memory size is equal to or larger than 25% of the maximum memory size supported

2) Run a series of 5 consecutive SERT runs using all elements of the new configuration

3) At most, 1 of the 5 runs can include one or more SERT *Group B Invalid* messages, as defined in Sub Clause 1.3.4.3.3

4) The coefficient of variation (CV) for each SERT worklet must be less than 10%

1.3.4.4.5 CPU Architecture Compliance Test Plan

Compliance for a new CPU architecture or CPU architecture portion can only be obtained with this test plan if the following is applicable:

Adding support for a new CPU architecture within a compliant CPU architecture class.

JVM and OS versions that have not yet been shown to be compliant for this CPU architecture class may be used and can gain compliance.

When testing a new CPU architecture for compliance, the tester must identify if all or only a portion of the CPU models sold of that architecture are being tested for compliance. Additionally, if the tester only desires to gain compliance for certain socket counts, this must be specified. This selection will affect the scope of the test plan and determine which CPUs and socket counts receive an entry in the Client Configuration XML file.

Test Plan:

1) CPU Socket Testing

a) Run SERT on the largest socket counts which is desired to be made compliant for this architecture or architecture portion. If the CPU architecture supports more than one socket type, test the largest socket count per CPU socket type. For this testing, all server CPU sockets shall be populated with CPUs.

b) If servers are sold in configurations with unpopulated CPU sockets, run SERT on these configurations.

Required outcomes:
For every test point, a SERT result with no *Group B Invalid Messages* (Sub Clause 1.3.4.3.3) must be completed

2) Memory Size Testing

a) For a selected configuration, test 2 supported memory sizes. If no platform of this CPU architecture supports more than 1 memory size, only complete test *b)*. The balanced memory requirement stated in Sub Clause 1.3.4.4.1 must be followed for all selected memory configurations.

b) A selected size equal to, or larger than, 25% of the max memory size supported. The selected size must be different from that selected in *c)*.

c) The second selected size shall be the larger of 8GB and the Minimum Balanced Memory Size for the selected server, as calculated in *Equation 11*.

Required outcome:
For every test point, a SERT result with no *Group B Invalid Messages* (Sub Clause 1.3.4.3.3) must be completed

3) CPU Core Count Testing

Run SERT on 2 CPUs with different core counts. If there are no CPU models of this architecture, or architecture portion, sold with 2 different core counts, only run with one core count. One of the core counts selected must be the maximum core count sold of this architecture, or architecture portion.

Required outcome:
For every test point, a SERT result with no *Group B Invalid Messages* (Sub Clause 1.3.4.3.3) must be completed

4) Validity and Variance Testing

Run a series of 5 consecutive SERT runs on a selected configuration

Required outcomes:
a) At most, 1 of the 5 runs can include one or more SERT *Group B Invalid* messages, as defined in Sub Clause 1.3.4.3.3

b) The coefficient of variation (CV) for each SERT worklet must be less than 10%

1.3.4.4.6 CPU Compliance Test Plan

Compliance for any new CPU architecture or CPU model can be obtained if the following test plan is successfully completed, even if no other CPU architectures in the same CPU architecture class have been shown to be compliant. In some situations, the reduced test plans of *Sub Clause 1.3.4.4.4* or *Sub Clause 1.3.4.4.5* may be applicable and can be used instead of this test plan.

When testing a new CPU architecture for compliance, the tester must identify if all or only a portion of the CPU models sold of that architecture are being tested for compliance. Additionally, if the tester only desires to gain compliance for certain socket counts, this must be specified. This selection will affect the scope of the test plan and determine which CPUs and socket counts receive an entry in the Client Configuration XML file.

Test Plan:

1) CPU Socket Testing

a) Run SERT on all socket counts which are desired to be made compliant for this architecture or architecture portion. For this testing, all server CPU sockets shall be populated with CPUs.

b) If servers are sold in configurations with unpopulated CPU sockets, run SERT on these configurations.

Required outcomes:
a) For every test point, a SERT result with no *Group B Invalid Messages* (Sub Clause 1.3.4.3.3) must be completed

b) For each server with more CPUs than the least supported, the 100% load level performance score of all CPU worklets, must be larger than the corresponding score from the run with fewer of the same model CPUs installed.

2) Memory Size Testing

a) For a selected configuration, test 2 supported memory sizes. If no platform of this CPU architecture, or architecture portion, supports more than 1 memory sizes, only complete tests *b)*. The balanced memory requirement stated in *Sub Clause 1.3.4.4.1* must be followed for all selected memory configurations.

b) A selected size equal to, or larger than, 50% of the max memory size supported. It is strongly encouraged to test the maximum size supported to ensure functionality across the entire range of supported memory sizes.

c) The second selected size shall be the larger of 8GB and the Minimum Balanced Memory Size for the selected server, as calculated in *Equation 11*.

Required outcome:
For every test point, a SERT result with no *Group B Invalid Messages* (Sub Clause 1.3.4.3.3) must be completed

3) Disk Quantity Testing

Run SERT on 3 different quantities of disks. If no platform of this CPU architecture, or architecture portion, supports 3 or more disks, run with the most different quantities supported. It is recommended to run with the maximum number of disks supported to ensure functionality across all disk controllers and connections.

Required outcome:
For every test point, a SERT result with no *Group B Invalid Messages* (Sub Clause 1.3.4.3.3) must be completed

4) CPU Core Count Testing

Run SERT on 2 CPUs with different core counts. If there are no CPU models of this architecture, or architecture portion, sold with 2 different core counts, only run with one core count. One of the core counts selected must be the maximum core count sold of this architecture, or architecture portion.

Required outcome:
For every test point, a SERT result with no *Group B Invalid Messages* (Sub Clause 1.3.4.3.3) must be completed

5) CPU Frequency Testing

Run SERT on 2 CPUs which are sold at different core frequencies. If there are not 2 CPU models of this architecture, or architecture portion, sold at different frequencies, run with only one CPU frequency. One of the frequencies selected must be the maximum frequency sold of this architecture, or architecture portion.

Required outcome:
For every test point, a SERT result with no *Group B Invalid Messages* (Sub Clause 1.3.4.3.3) must be completed

6) Memory Frequency Testing

Run SERT on 2 different memory frequencies. If no platform of this CPU architecture, or architecture portion, supports 2 different memory frequencies, run at one memory frequency.

Required outcome:

For every test point, a SERT result with no *Group B Invalid Messages* (Sub Clause 1.3.4.3.3) must be completed

7) Storage Technology Testing

Run SERT with 2 different storage devices using different technologies, for example HDDs and SSDs. If no platform of this CPU architecture, or architecture portion, supports 2 different types of storage technologies, run with only 1 type of disk. If the only storage devices supported are HDDs, test with two different rotational speeds, and only one speed if two rotation speeds are not supported.

Required outcome:
For every test point, a SERT result with no *Group B Invalid Messages* (Sub Clause 1.3.4.3.3) must be completed

8) Validity and Variance Testing

Run a series of 5 consecutive SERT runs on a selected configuration

Required outcomes:
a) At most, 1 of the 5 runs can include one or more SERT *Group B Invalid Messages*, as defined in *Sub Clause 1.3.4.3.3*

b) The coefficient of variation (CV) for each SERT worklet must be less than 10%

1.3.5 Power Analysers

1.3.5.1 *Introduction*

A list of power analysers which meet the requirements of this sub clause is available in *Annex B*. Included in this sub clause is a set of general requirements, two test plans to verify a power analyser's accuracy, and an additional test plan related to the power requirements of a given SUT to be tested. In order to use a new power analyser with SERT, software support for the new power analyser must be added to the PTDaemon tool. The SPEC process to add this support is available at http://spec.org/power/docs/SPEC-Power_Analyzer_Acceptance_Process.pdf. The SPEC adoption process may include additional requirements to those described in these Sub Clauses.

1.3.5.2 *General Power Analyser Requirements*

The list of power analysers that have already been shown to comply with these requirements are listed in Annex B. Additional power analysers can be used only if they have been shown to satisfy all of the following requirements:

1. Measurements - the analyser must report true RMS power (watts) and at least two of the following measurement units: voltage, amps or power factor.

2. Measurements must be reported by the analyser with an overall uncertainty of 1% or better during all sections of the Pulse Acceptance Test, defined in Sub Clause 1.3.5.3.

3. Calibration - the analyser must be able to be calibrated by a standard traceable to NIST (U.S.A.) (http://nist.gov) or a counterpart national metrology institute in other countries.

4. Crest Factor - The analyser must provide a current crest factor of a minimum value of 3. For power analysers which do not specify the crest factor, the analyser must be capable of

measuring an amperage spike of at least 3 times the maximum amperage used in the Pulse Acceptance Test, defined in Sub Clause 1.3.5.3.

5. Logging - The analyser must support reading data in real time, using a documented software interface. If a software package is required to access this interface, this software must be available to all users of the device, or freely available and redistributable. Analysers must support a reading rate of at least 1 set of measurements per second. The measurement set must include watts and at least two of, volts, amps, and power factor. The data averaging interval of the analyser must be 1 (preferred) or 2 times the reading interval.

1.3.5.3 *Simultaneous Measurements Test*

To verify the measurement accuracy of a power analyser not included in *Annex B*, the following test must be performed and the specified result must be achieved.

1. Select a SUT, a power analyser from the list in *Annex B*, and a new power analyser to be tested.
2. Ensure the new power analyser satisfies all the requirements of *Sub Clause 1.3.5.2*.
3. Connect the new power analyser and the power analyser from *Annex B*, in series, between the SUT and the power source (in either order).
4. Configure and run SERT.
5. Reverse the order of the power analysers, so the opposite analyser is now connected to the SUT. This step is intended to eliminate any measurement differences due to voltage drops or power consumption of the analysers themselves.
6. Rerun the SERT test.
7. Per load level of each SERT worklet, the difference between the average power values from the two power analysers shall not be larger than, the sum of the uncertainties of each power analyser at each measured power level. Note, these uncertainties are calculated by PTDaemon as a convenience to the tester.

1.3.5.4 *Pulse Acceptance Test*

To verify the measurement accuracy of a power analyser not included in the list in *Annex B*, the following test must be performed and the specified result achieved.

1. Configure a hardware or software programmable load generator to generate 10 pulses each, of 100 to 900 ms in 100ms steps, starting every 5000ms. Baseline load must be between 40 watts and 150 watts within one of the allowed voltage ranges. The pulses must reach at least 20% higher than the baseline.

2. Measure the pulses with the power analyser being evaluated.

3. All measured power values must correspond to the pulse widths generated by the load generator, within a tolerance of ±25%. All pulses must be captured by the power analyser.

4. Reconfigure the load generator to generate 100 100ms pulses starting at 5010ms intervals, followed by 100 200ms pulses starting every 5010ms.

5. Measure the pulses with the power analyser being evaluated.

6. The power analyser must indicate all pulses, with two exceptions. It is allowed to indicate up to two duplicate sample reading and two missing sample readings. A duplicate sample reading is when the power analyser indicates two pulses occurred when the load generator only generated one pulse.

1.3.5.5 *Server Specific Power Analyser Requirements*

There are many different sizes and types of servers which have differing power requirements. In addition to the General Power Analyser Requirements of *Sub Clause 1.3.5.2*, there are also requirements that the power analyser has sufficient accuracy in the ranges used by the SUT.

When running SERT on a SUT, using an allowed frequency and voltage, the power analyser must provide an uncertainty under 1% and a crest factor of 3 or more, for loads with a power factor between 0.8 and 1.0, and wattages from 20W to the maximum used in a SERT run on the SUT.

1.3.6 Temperature Sensors

A list of temperature sensors which meet the requirements of this sub clause is available in *Annex B*. In order to use a new temperature sensor with SERT, software support for the new sensor must be added to the PTDaemon tool. The SPEC process to add this support is available at http://spec.org/power/docs/SPEC-Power_Analyzer_Acceptance_Process.pdf. The SPEC adoption process may include additional requirements to those described in these Sub Clauses.

All temperature sensors used in SEEM must meet all of the following requirements:

1. Logging – The sensor must support reading data in real time, using a documented software interface. If a software package is required to access this interface, this software must be available to all users of the device, or freely available and redistributable. The reading rate supported by the sensor must be at least 4 samples per minute.

2. Accuracy - Measurements must be reported by the sensor with an overall accuracy of ±0.5° Celsius (C) or better for temperatures between 20°C and 50°C.

Annex A: Approved CPU Architectures, Operating Systems, and Java Virtual Machines

The following list of sets of CPUs, Operating Systems, and JVMs are approved for use with SEEM. Only CPUs, OSes and JVMs from the same set (a row in the below table) are approved for use together in SEEM. Unless otherwise noted, OSes and JVM updates and patches of the same version stated in the table, are also approved. Additional CPU, OS, JVM sets can only be used with SEEM if they meet all the requirements of Sub Clause 1.3.4. Detailed settings for each configuration is available at https://www.spec.org/sert2/SERT-JVM_Options-2.0.html or the link included in the *Configuration* column. Additionally, the settings are included as part of SERT 2.0.1 release.

CPU Vendor	CPU Model(s)	Operating System	JVM	Configuration
Intel	E3-XXXX	Windows Server 2008 R2 SP1	HotSpot 1.7.0	Intel_Win_HS17_1n
Intel	E3-XXXX	Windows Server 2012	HotSpot 1.7.0	Intel_Win_HS17_1n
Intel	E3-XXXX	Windows Server 2012 R2	HotSpot 1.7.0	Intel_Win_HS17_1n
Intel	E5-XXXX	Windows Server 2008 R2 SP1	HotSpot 1.7.0	Intel_Win_HS17_1n
Intel	E5-XXXX	Windows Server 2012	HotSpot 1.7.0	Intel_Win_HS17_1n
Intel	E5-XXXX	Windows Server 2012 R2	HotSpot 1.7.0	Intel_Win_HS17_1n
Intel	E3-XXXX v2	Windows Server 2008 R2 SP1	HotSpot 1.7.0	Intel_Win_HS17_1n
Intel	E3-XXXX v2	Windows Server 2012	HotSpot 1.7.0	Intel_Win_HS17_1n
Intel	E3-XXXX v2	Windows Server 2012 R2	HotSpot 1.7.0	Intel_Win_HS17_1n
Intel	E5-XXXX v2	Windows Server 2008 R2 SP1	HotSpot 1.7.0	Intel_Win_HS17_1n
Intel	E5-XXXX v2	Windows Server 2012	HotSpot 1.7.0	Intel_Win_HS17_1n
Intel	E5-XXXX v2	Windows Server 2012 R2	HotSpot 1.7.0	Intel_Win_HS17_1n
Intel	E3-XXXX v3	Windows Server 2008 R2 SP1	HotSpot 1.7.0	Intel_Win_HS17_1n
Intel	E3-XXXX v3	Windows Server 2012	HotSpot 1.7.0	Intel_Win_HS17_1n
Intel	E3-XXXX v3	Windows Server 2012 R2	HotSpot 1.7.0	Intel_Win_HS17_1n
Intel	E5-XXXX v3	Windows Server 2008 R2 SP1	HotSpot 1.7.0	Intel_Win_HS17_1n
Intel	E5-XXXX v3	Windows Server 2012	HotSpot 1.7.0	Intel_Win_HS17_1n
Intel	E5-XXXX v3	Windows Server 2012 R2	HotSpot 1.7.0	Intel_Win_HS17_1n
Intel	E3-XXXX v4	Windows Server 2012 R2	HotSpot 1.7.0	Intel_Win_HS17_1n
Intel	E3-XXXX v5	Windows Server 2012 R2	HotSpot 1.7.0	Intel_Win_HS17_1n
Intel	E3-XXXX v3	Windows Server 2012 R2	HotSpot 1.8.0 pre121	Intel_Win_HS18_1
Intel	E3-XXXX v3	Windows Server 2012 R2	HotSpot 1.8.0 post120	Intel_Win_HS18_1

Intel	E5-XXXX v3	Windows Server 2012 R2	HotSpot 1.8.0 pre121	Intel_Win_HS18_1
Intel	E5-XXXX v3	Windows Server 2012 R2	HotSpot 1.8.0 post120	Intel_Win_HS18_1
Intel	E3-XXXX v4	Windows Server 2012 R2	HotSpot 1.8.0 pre121	Intel_Win_HS18_2
Intel	E3-XXXX v4	Windows Server 2012 R2	HotSpot 1.8.0 post120	Intel_Win_HS18_2
Intel	E5-XXXX v4	Windows Server 2012 R2	HotSpot 1.8.0 pre121	Intel_Win_HS18_3
Intel	E7-XXXX v4	Windows Server 2012 R2	HotSpot 1.8.0 pre121	Intel_Win_HS18_3
Intel	E5-XXXX v4	Windows Server 2012 R2	HotSpot 1.8.0 post120	Intel_Win_HS18_4
Intel	E7-XXXX v4	Windows Server 2012 R2	HotSpot 1.8.0 post120	Intel_Win_HS18_4
Intel	Xeon Platinum	Windows Server 2012 R2	HotSpot 1.8.0 pre121	Intel_Win_HS18_5
Intel	Xeon Platinum	Windows Server 2012 R2	HotSpot 1.8.0 post120	Intel_Win_HS18_5
Intel	Xeon Gold	Windows Server 2012 R2	HotSpot 1.8.0 pre121	Intel_Win_HS18_5
Intel	Xeon Gold	Windows Server 2012 R2	HotSpot 1.8.0 post120	Intel_Win_HS18_5
Intel	Xeon Silver	Windows Server 2012 R2	HotSpot 1.8.0 pre121	Intel_Win_HS18_5
Intel	Xeon Silver	Windows Server 2012 R2	HotSpot 1.8.0 post120	Intel_Win_HS18_5
Intel	Xeon Bronze	Windows Server 2012 R2	HotSpot 1.8.0 pre121	Intel_Win_HS18_5
Intel	Xeon Bronze	Windows Server 2012 R2	HotSpot 1.8.0 post120	Intel_Win_HS18_5
Intel	E3-XXXX	Windows Server 2008 R2 SP1	J9 1.7.0 SR1	Intel_Win_J917_1dyn
Intel	E3-XXXX	Windows Server 2008 R2 SP1	J9 1.7.0 SR2	Intel_Win_J917_1dyn
Intel	E5-XXXX	Windows Server 2008 R2 SP1	J9 1.7.0 SR1	Intel_Win_J917_1dyn
Intel	E5-XXXX	Windows Server 2008 R2 SP1	J9 1.7.0 SR2	Intel_Win_J917_1dyn
Intel	E3-XXXX v2	Windows Server 2008 R2 SP1	J9 1.7.0 SR1	Intel_Win_J917_1dyn
Intel	E3-XXXX v2	Windows Server 2008 R2 SP1	J9 1.7.0 SR2	Intel_Win_J917_1dyn
Intel	E5-XXXX v2	Windows Server 2008 R2 SP1	J9 1.7.0 SR1	Intel_Win_J917_1dyn
Intel	E5-XXXX v2	Windows Server 2008 R2 SP1	J9 1.7.0 SR2	Intel_Win_J917_1dyn
Intel	E3-XXXX	Windows Server 2008 R2 SP1	J9 1.7.0 SR3	Intel_Win_J917_3dyn
Intel	E3-XXXX	Windows Server 2008 R2 SP1	J9 1.7.0 SR6	Intel_Win_J917_3dyn
Intel	E5-XXXX	Windows Server 2008 R2 SP1	J9 1.7.0 SR3	Intel_Win_J917_3dyn
Intel	E5-XXXX	Windows Server 2008 R2 SP1	J9 1.7.0 SR6	Intel_Win_J917_3dyn
Intel	E3-XXXX v2	Windows Server 2008 R2 SP1	J9 1.7.0 SR3	Intel_Win_J917_3dyn
Intel	E3-XXXX v2	Windows Server 2008 R2 SP1	J9 1.7.0 SR6	Intel_Win_J917_3dyn
Intel	E5-XXXX v2	Windows Server 2008 R2 SP1	J9 1.7.0 SR3	Intel_Win_J917_3dyn
Intel	E5-XXXX v2	Windows Server 2008 R2 SP1	J9 1.7.0 SR6	Intel_Win_J917_3dyn

Intel	E3-XXXX v3	Windows Server 2008 R2 SP1	J9 1.7.0 SR3	Intel_Win_J917_3dyn
Intel	E3-XXXX v3	Windows Server 2008 R2 SP1	J9 1.7.0 SR6	Intel_Win_J917_3dyn
Intel	E5-XXXX v3	Windows Server 2008 R2 SP1	J9 1.7.0 SR3	Intel_Win_J917_3dyn
Intel	E5-XXXX v3	Windows Server 2008 R2 SP1	J9 1.7.0 SR6	Intel_Win_J917_3dyn
Intel	E3-XXXX	Windows Server 2012	J9 1.7.0 SR6	Intel_Win_J917_3dyn
Intel	E3-XXXX	Windows Server 2012 R2	J9 1.7.0 SR6	Intel_Win_J917_3dyn
Intel	E5-XXXX	Windows Server 2012	J9 1.7.0 SR6	Intel_Win_J917_3dyn
Intel	E5-XXXX	Windows Server 2012 R2	J9 1.7.0 SR6	Intel_Win_J917_3dyn
Intel	E3-XXXX v2	Windows Server 2012	J9 1.7.0 SR6	Intel_Win_J917_3dyn
Intel	E3-XXXX v2	Windows Server 2012 R2	J9 1.7.0 SR6	Intel_Win_J917_3dyn
Intel	E5-XXXX v2	Windows Server 2012	J9 1.7.0 SR6	Intel_Win_J917_3dyn
Intel	E5-XXXX v2	Windows Server 2012 R2	J9 1.7.0 SR6	Intel_Win_J917_3dyn
Intel	E3-XXXX v3	Windows Server 2012	J9 1.7.0 SR6	Intel_Win_J917_3dyn
Intel	E3-XXXX v3	Windows Server 2012 R2	J9 1.7.0 SR6	Intel_Win_J917_3dyn
Intel	E5-XXXX v3	Windows Server 2012	J9 1.7.0 SR6	Intel_Win_J917_3dyn
Intel	E5-XXXX v3	Windows Server 2012 R2	J9 1.7.0 SR6	Intel_Win_J917_3dyn
Intel	E3-XXXX	Red Hat Enterprise Linux Server 6	HotSpot 1.7.0	Intel_Lin_HS17_1n
Intel	E3-XXXX	SUSE Linux Enterprise Server 11	HotSpot 1.7.0	Intel_Lin_HS17_1n
Intel	E3-XXXX	Oracle Linux 6	HotSpot 1.7.0	Intel_Lin_HS17_1n
Intel	E5-XXXX	Red Hat Enterprise Linux Server 6	HotSpot 1.7.0	Intel_Lin_HS17_1n
Intel	E5-XXXX	SUSE Linux Enterprise Server 11	HotSpot 1.7.0	Intel_Lin_HS17_1n
Intel	E5-XXXX	Oracle Linux 6	HotSpot 1.7.0	Intel_Lin_HS17_1n
Intel	E3-XXXX v2	Red Hat Enterprise Linux Server 6	HotSpot 1.7.0	Intel_Lin_HS17_1n
Intel	E3-XXXX v2	SUSE Linux Enterprise Server 11	HotSpot 1.7.0	Intel_Lin_HS17_1n
Intel	E3-XXXX v2	Oracle Linux 6	HotSpot 1.7.0	Intel_Lin_HS17_1n
Intel	E5-XXXX v2	Red Hat Enterprise Linux Server 6	HotSpot 1.7.0	Intel_Lin_HS17_1n
Intel	E5-XXXX v2	SUSE Linux Enterprise Server 11	HotSpot 1.7.0	Intel_Lin_HS17_1n
Intel	E5-XXXX v2	Oracle Linux 6	HotSpot 1.7.0	Intel_Lin_HS17_1n
Intel	E3-XXXX	Red Hat Enterprise Linux Server 7	HotSpot 1.7.0	Intel_Lin_HS17_2n

Intel	E5-XXXX	Red Hat Enterprise Linux Server 7	HotSpot 1.7.0	Intel_Lin_HS17_2n
Intel	E3-XXXX v2	Red Hat Enterprise Linux Server 7	HotSpot 1.7.0	Intel_Lin_HS17_2n
Intel	E5-XXXX v2	Red Hat Enterprise Linux Server 7	HotSpot 1.7.0	Intel_Lin_HS17_2n
Intel	E3-XXXX v3	Red Hat Enterprise Linux Server 7	HotSpot 1.7.0	Intel_Lin_HS17_2n
Intel	E5-XXXX v3	Red Hat Enterprise Linux Server 7	HotSpot 1.7.0	Intel_Lin_HS17_2n
Intel	E7-XXXX v3	Red Hat Enterprise Linux Server 7	HotSpot 1.7.0	Intel_Lin_HS17_2n
Intel	E3-XXXX v3	SUSE Linux Enterprise Server 11	HotSpot 1.7.0	Intel_Lin_HS17_2n
Intel	E5-XXXX v3	SUSE Linux Enterprise Server 11	HotSpot 1.7.0	Intel_Lin_HS17_2n
Intel	E5-XXXX v4	Red Hat Enterprise Linux Server 7	HotSpot 1.8.0 pre121	Intel_Lin_HS18_1
Intel	E5-XXXX v4	Red Hat Enterprise Linux Server 7	HotSpot 1.8.0 post120	Intel_Lin_HS18_1
Intel	E5-XXXX v4	Red Hat Enterprise Linux Server 7	OpenJDK 1.8.0	Intel_Lin_HS18_1
Intel	E7-XXXX v4	Red Hat Enterprise Linux Server 7	HotSpot 1.8.0 pre121	Intel_Lin_HS18_1
Intel	E7-XXXX v4	Red Hat Enterprise Linux Server 7	HotSpot 1.8.0 post120	Intel_Lin_HS18_1
Intel	E7-XXXX v4	Red Hat Enterprise Linux Server 7	OpenJDK 1.8.0	Intel_Lin_HS18_1
Intel	Xeon Platinum	Red Hat Enterprise Linux Server 7	HotSpot 1.8.0 pre121	Intel_Lin_HS18_2
Intel	Xeon Platinum	Red Hat Enterprise Linux Server 7	HotSpot 1.8.0 post120	Intel_Lin_HS18_2
Intel	Xeon Platinum	Red Hat Enterprise Linux Server 7	OpenJDK 1.8.0	Intel_Lin_HS18_2
Intel	Xeon Gold	Red Hat Enterprise Linux Server 7	HotSpot 1.8.0 pre121	Intel_Lin_HS18_2
Intel	Xeon Gold	Red Hat Enterprise Linux Server 7	HotSpot 1.8.0 post120	Intel_Lin_HS18_2
Intel	Xeon Gold	Red Hat Enterprise Linux Server 7	OpenJDK 1.8.0	Intel_Lin_HS18_2
Intel	Xeon Silver	Red Hat Enterprise Linux Server 7	HotSpot 1.8.0 pre121	Intel_Lin_HS18_2
Intel	Xeon Silver	Red Hat Enterprise Linux Server 7	HotSpot 1.8.0 post120	Intel_Lin_HS18_2
Intel	Xeon Silver	Red Hat Enterprise Linux Server 7	OpenJDK 1.8.0	Intel_Lin_HS18_2
Intel	Xeon Bronze	Red Hat Enterprise Linux Server 7	HotSpot 1.8.0 pre121	Intel_Lin_HS18_2
Intel	Xeon Bronze	Red Hat Enterprise Linux Server 7	HotSpot 1.8.0 post120	Intel_Lin_HS18_2

Intel	Xeon Bronze	Red Hat Enterprise Linux Server 7	OpenJDK 1.8.0	Intel_Lin_HS18_2
Intel	E3-XXXX	Red Hat Enterprise Linux Server 6	J9 1.7.0 SR1	Intel_Lin_J917_1dyn
Intel	E3-XXXX	Red Hat Enterprise Linux Server 6	J9 1.7.0 SR2	Intel_Lin_J917_1dyn
Intel	E3-XXXX	Red Hat Enterprise Linux Server 6	J9 1.7.0 SR3	Intel_Lin_J917_1dyn
Intel	E3-XXXX	Red Hat Enterprise Linux Server 6	J9 1.7.0 SR6	Intel_Lin_J917_1dyn
Intel	E3-XXXX	SUSE Linux Enterprise Server 11	J9 1.7.0 SR1	Intel_Lin_J917_1dyn
Intel	E3-XXXX	SUSE Linux Enterprise Server 11	J9 1.7.0 SR2	Intel_Lin_J917_1dyn
Intel	E3-XXXX	SUSE Linux Enterprise Server 11	J9 1.7.0 SR3	Intel_Lin_J917_1dyn
Intel	E3-XXXX	SUSE Linux Enterprise Server 11	J9 1.7.0 SR6	Intel_Lin_J917_1dyn
Intel	E3-XXXX	Oracle Linux 6	J9 1.7.0 SR1	Intel_Lin_J917_1dyn
Intel	E3-XXXX	Oracle Linux 6	J9 1.7.0 SR2	Intel_Lin_J917_1dyn
Intel	E3-XXXX	Oracle Linux 6	J9 1.7.0 SR3	Intel_Lin_J917_1dyn
Intel	E3-XXXX	Oracle Linux 6	J9 1.7.0 SR6	Intel_Lin_J917_1dyn
Intel	E5-XXXX	Red Hat Enterprise Linux Server 6	J9 1.7.0 SR1	Intel_Lin_J917_1dyn
Intel	E5-XXXX	Red Hat Enterprise Linux Server 6	J9 1.7.0 SR2	Intel_Lin_J917_1dyn
Intel	E5-XXXX	Red Hat Enterprise Linux Server 6	J9 1.7.0 SR3	Intel_Lin_J917_1dyn
Intel	E5-XXXX	Red Hat Enterprise Linux Server 6	J9 1.7.0 SR6	Intel_Lin_J917_1dyn
Intel	E5-XXXX	SUSE Linux Enterprise Server 11	J9 1.7.0 SR1	Intel_Lin_J917_1dyn
Intel	E5-XXXX	SUSE Linux Enterprise Server 11	J9 1.7.0 SR2	Intel_Lin_J917_1dyn
Intel	E5-XXXX	SUSE Linux Enterprise Server 11	J9 1.7.0 SR3	Intel_Lin_J917_1dyn
Intel	E5-XXXX	SUSE Linux Enterprise Server 11	J9 1.7.0 SR6	Intel_Lin_J917_1dyn
Intel	E5-XXXX	Oracle Linux 6	J9 1.7.0 SR1	Intel_Lin_J917_1dyn
Intel	E5-XXXX	Oracle Linux 6	J9 1.7.0 SR2	Intel_Lin_J917_1dyn
Intel	E5-XXXX	Oracle Linux 6	J9 1.7.0 SR3	Intel_Lin_J917_1dyn
Intel	E5-XXXX	Oracle Linux 6	J9 1.7.0 SR6	Intel_Lin_J917_1dyn

Intel	E3-XXXX v2	Red Hat Enterprise Linux Server 6	J9 1.7.0 SR1	Intel_Lin_J917_1dyn
Intel	E3-XXXX v2	Red Hat Enterprise Linux Server 6	J9 1.7.0 SR2	Intel_Lin_J917_1dyn
Intel	E3-XXXX v2	Red Hat Enterprise Linux Server 6	J9 1.7.0 SR3	Intel_Lin_J917_1dyn
Intel	E3-XXXX v2	Red Hat Enterprise Linux Server 6	J9 1.7.0 SR6	Intel_Lin_J917_1dyn
Intel	E3-XXXX v2	SUSE Linux Enterprise Server 11	J9 1.7.0 SR1	Intel_Lin_J917_1dyn
Intel	E3-XXXX v2	SUSE Linux Enterprise Server 11	J9 1.7.0 SR2	Intel_Lin_J917_1dyn
Intel	E3-XXXX v2	SUSE Linux Enterprise Server 11	J9 1.7.0 SR3	Intel_Lin_J917_1dyn
Intel	E3-XXXX v2	SUSE Linux Enterprise Server 11	J9 1.7.0 SR6	Intel_Lin_J917_1dyn
Intel	E3-XXXX v2	Oracle Linux 6	J9 1.7.0 SR1	Intel_Lin_J917_1dyn
Intel	E3-XXXX v2	Oracle Linux 6	J9 1.7.0 SR2	Intel_Lin_J917_1dyn
Intel	E3-XXXX v2	Oracle Linux 6	J9 1.7.0 SR3	Intel_Lin_J917_1dyn
Intel	E3-XXXX v2	Oracle Linux 6	J9 1.7.0 SR6	Intel_Lin_J917_1dyn
Intel	E5-XXXX v2	Red Hat Enterprise Linux Server 6	J9 1.7.0 SR1	Intel_Lin_J917_1dyn
Intel	E5-XXXX v2	Red Hat Enterprise Linux Server 6	J9 1.7.0 SR2	Intel_Lin_J917_1dyn
Intel	E5-XXXX v2	Red Hat Enterprise Linux Server 6	J9 1.7.0 SR3	Intel_Lin_J917_1dyn
Intel	E5-XXXX v2	Red Hat Enterprise Linux Server 6	J9 1.7.0 SR6	Intel_Lin_J917_1dyn
Intel	E5-XXXX v2	SUSE Linux Enterprise Server 11	J9 1.7.0 SR1	Intel_Lin_J917_1dyn
Intel	E5-XXXX v2	SUSE Linux Enterprise Server 11	J9 1.7.0 SR2	Intel_Lin_J917_1dyn
Intel	E5-XXXX v2	SUSE Linux Enterprise Server 11	J9 1.7.0 SR3	Intel_Lin_J917_1dyn
Intel	E5-XXXX v2	SUSE Linux Enterprise Server 11	J9 1.7.0 SR6	Intel_Lin_J917_1dyn
Intel	E5-XXXX v2	Oracle Linux 6	J9 1.7.0 SR1	Intel_Lin_J917_1dyn
Intel	E5-XXXX v2	Oracle Linux 6	J9 1.7.0 SR2	Intel_Lin_J917_1dyn
Intel	E5-XXXX v2	Oracle Linux 6	J9 1.7.0 SR3	Intel_Lin_J917_1dyn
Intel	E5-XXXX v2	Oracle Linux 6	J9 1.7.0 SR6	Intel_Lin_J917_1dyn
Intel	E7-4XXX	Red Hat Enterprise Linux Server 6	J9 1.7.0 SR1	Intel_Lin_J917_1dyn
Intel	E7-4XXX	Red Hat Enterprise Linux Server 6	J9 1.7.0 SR2	Intel_Lin_J917_1dyn
Intel	E7-4XXX	Red Hat Enterprise Linux Server 6	J9 1.7.0 SR3	Intel_Lin_J917_1dyn
Intel	E7-4XXX	Red Hat Enterprise Linux Server 6	J9 1.7.0 SR6	Intel_Lin_J917_1dyn
Intel	E7-4XXX	SUSE Linux Enterprise Server 11	J9 1.7.0 SR1	Intel_Lin_J917_1dyn

Intel	E7-4XXX	SUSE Linux Enterprise Server 11	J9 1.7.0 SR2	Intel_Lin_J917_1dyn
Intel	E7-4XXX	SUSE Linux Enterprise Server 11	J9 1.7.0 SR3	Intel_Lin_J917_1dyn
Intel	E7-4XXX	SUSE Linux Enterprise Server 11	J9 1.7.0 SR6	Intel_Lin_J917_1dyn
Intel	E7-4XXX	Oracle Linux 6	J9 1.7.0 SR1	Intel_Lin_J917_1dyn
Intel	E7-4XXX	Oracle Linux 6	J9 1.7.0 SR2	Intel_Lin_J917_1dyn
Intel	E7-4XXX	Oracle Linux 6	J9 1.7.0 SR3	Intel_Lin_J917_1dyn
Intel	E7-4XXX	Oracle Linux 6	J9 1.7.0 SR6	Intel_Lin_J917_1dyn
Intel	E3-XXXX v2	Solaris 11	HotSpot 1.7.0	Intel_Sol_HS17_1
Intel	E5-XXXX v2	Solaris 11	HotSpot 1.7.0	Intel_Sol_HS17_1
Intel	E7-XXXX v2	Windows Server 2008 R2 SP1	HotSpot 1.7.0	Intel_Win_HS17_2n
Intel	E7-4XXX	Windows Server 2008 R2 SP1	HotSpot 1.7.0	Intel_Win_HS17_2n
Intel	E7-XXXX v3	Windows Server 2008 R2 SP1	HotSpot 1.7.0	Intel_Win_HS17_3n
Intel	E7-XXXX v3	Windows Server 2012 R2	HotSpot 1.7.0	Intel_Win_HS17_3n
Intel	E5-XXXX v4	Windows Server 2012 R2	HotSpot 1.7.0	Intel_Win_HS17_3n
Intel	E7-4XXX	Windows Server 2008 R2 SP1	J9 1.7.0 SR1	Intel_Win_J917_2dyn
Intel	E7-4XXX	Windows Server 2008 R2 SP1	J9 1.7.0 SR2	Intel_Win_J917_2dyn
Intel	E7-4XXX	Windows Server 2008 R2 SP1	J9 1.7.0 SR3	Intel_Win_J917_2dyn
Intel	E7-4XXX	Windows Server 2008 R2 SP1	J9 1.7.0 SR6	Intel_Win_J917_2dyn
Intel	E7-XXXX v2	Windows Server 2012 R2	J9 1.7.0 SR6	Intel_Win_J917_3dyn
Intel	E7-XXXX v2	Red Hat Enterprise Linux Server 6	HotSpot 1.7.0	Intel_Lin_HS17_1n
Intel	E7-XXXX v2	SUSE Linux Enterprise Server 11	HotSpot 1.7.0	Intel_Lin_HS17_1n
Intel	E7-XXXX v2	Oracle Linux 6	HotSpot 1.7.0	Intel_Lin_HS17_1n
Intel	E7-4XXX	Red Hat Enterprise Linux Server 6	HotSpot 1.7.0	Intel_Lin_HS17_1n
Intel	E7-4XXX	SUSE Linux Enterprise Server 11	HotSpot 1.7.0	Intel_Lin_HS17_1n
Intel	E7-4XXX	Oracle Linux 6	HotSpot 1.7.0	Intel_Lin_HS17_1n
AMD	EPYC 7xxx	Windows Server 2012 R2	HotSpot 1.8.0 post120	AMD_EPYC_Win_HS18_1
AMD	Opteron 32xx	Windows Server 2008 R2 SP1	HotSpot 1.7.0	AMD_Win_HS17_1

AMD	Opteron 32xx	Windows Server 2012 R2	HotSpot 1.7.0	AMD_Win_HS17_1
AMD	Opteron 41xx	Windows Server 2008 R2 SP1	HotSpot 1.7.0	AMD_Win_HS17_1
AMD	Opteron 41xx	Windows Server 2012 R2	HotSpot 1.7.0	AMD_Win_HS17_1
AMD	Opteron 42xx	Windows Server 2008 R2 SP1	HotSpot 1.7.0	AMD_Win_HS17_1
AMD	Opteron 42xx	Windows Server 2012 R2	HotSpot 1.7.0	AMD_Win_HS17_1
AMD	Opteron 43xx	Windows Server 2008 R2 SP1	HotSpot 1.7.0	AMD_Win_HS17_1
AMD	Opteron 43xx	Windows Server 2012 R2	HotSpot 1.7.0	AMD_Win_HS17_1
AMD	Opteron 61xx	Windows Server 2008 R2 SP1	HotSpot 1.7.0	AMD_Win_HS17_1
AMD	Opteron 61xx	Windows Server 2012 R2	HotSpot 1.7.0	AMD_Win_HS17_1
AMD	Opteron 62xx	Windows Server 2008 R2 SP1	HotSpot 1.7.0	AMD_Win_HS17_1
AMD	Opteron 62xx	Windows Server 2012 R2	HotSpot 1.7.0	AMD_Win_HS17_1
AMD	Opteron 63xx	Windows Server 2008 R2 SP1	HotSpot 1.7.0	AMD_Win_HS17_1
AMD	Opteron 63xx	Windows Server 2012 R2	HotSpot 1.7.0	AMD_Win_HS17_1
AMD	Opteron 32xx	Red Hat Enterprise Linux Server 6	HotSpot 1.7.0	AMD_Lin_HS17_1
AMD	Opteron 32xx	SUSE Linux Enterprise Server 11	HotSpot 1.7.0	AMD_Lin_HS17_1
AMD	Opteron 32xx	Oracle Linux 6	HotSpot 1.7.0	AMD_Lin_HS17_1
AMD	Opteron 41xx	Red Hat Enterprise Linux Server 6	HotSpot 1.7.0	AMD_Lin_HS17_1
AMD	Opteron 41xx	SUSE Linux Enterprise Server 11	HotSpot 1.7.0	AMD_Lin_HS17_1
AMD	Opteron 41xx	Oracle Linux 6	HotSpot 1.7.0	AMD_Lin_HS17_1
AMD	Opteron 42xx	Red Hat Enterprise Linux Server 6	HotSpot 1.7.0	AMD_Lin_HS17_1
AMD	Opteron 42xx	SUSE Linux Enterprise Server 11	HotSpot 1.7.0	AMD_Lin_HS17_1
AMD	Opteron 42xx	Oracle Linux 6	HotSpot 1.7.0	AMD_Lin_HS17_1
AMD	Opteron 43xx	Red Hat Enterprise Linux Server 6	HotSpot 1.7.0	AMD_Lin_HS17_1
AMD	Opteron 43xx	SUSE Linux Enterprise Server 11	HotSpot 1.7.0	AMD_Lin_HS17_1
AMD	Opteron 43xx	Oracle Linux 6	HotSpot 1.7.0	AMD_Lin_HS17_1
AMD	Opteron 61xx	Red Hat Enterprise Linux Server 6	HotSpot 1.7.0	AMD_Lin_HS17_1
AMD	Opteron 61xx	SUSE Linux Enterprise Server 11	HotSpot 1.7.0	AMD_Lin_HS17_1
AMD	Opteron 61xx	Oracle Linux 6	HotSpot 1.7.0	AMD_Lin_HS17_1
AMD	Opteron 62xx	Red Hat Enterprise Linux Server 6	HotSpot 1.7.0	AMD_Lin_HS17_1
AMD	Opteron 62xx	SUSE Linux Enterprise Server 11	HotSpot 1.7.0	AMD_Lin_HS17_1
AMD	Opteron 62xx	Oracle Linux 6	HotSpot 1.7.0	AMD_Lin_HS17_1
AMD	Opteron 63xx	Red Hat Enterprise Linux Server 6	HotSpot 1.7.0	AMD_Lin_HS17_1

AMD	Opteron 63xx	SUSE Linux Enterprise Server 11	HotSpot 1.7.0	AMD_Lin_HS17_1
AMD	Opteron 63xx	Oracle Linux 6	HotSpot 1.7.0	AMD_Lin_HS17_1
AMD	Opteron 32xx	Windows Server 2008 R2 SP1	J9 1.7.0 SR1	AMD_Win_J917_1dyn
AMD	Opteron 32xx	Windows Server 2008 R2 SP1	J9 1.7.0 SR2	AMD_Win_J917_1dyn
AMD	Opteron 41xx	Windows Server 2008 R2 SP1	J9 1.7.0 SR1	AMD_Win_J917_1dyn
AMD	Opteron 41xx	Windows Server 2008 R2 SP1	J9 1.7.0 SR2	AMD_Win_J917_1dyn
AMD	Opteron 42xx	Windows Server 2008 R2 SP1	J9 1.7.0 SR1	AMD_Win_J917_1dyn
AMD	Opteron 42xx	Windows Server 2008 R2 SP1	J9 1.7.0 SR2	AMD_Win_J917_1dyn
AMD	Opteron 43xx	Windows Server 2008 R2 SP1	J9 1.7.0 SR1	AMD_Win_J917_1dyn
AMD	Opteron 43xx	Windows Server 2008 R2 SP1	J9 1.7.0 SR2	AMD_Win_J917_1dyn
AMD	Opteron 61xx	Windows Server 2008 R2 SP1	J9 1.7.0 SR1	AMD_Win_J917_1dyn
AMD	Opteron 61xx	Windows Server 2008 R2 SP1	J9 1.7.0 SR2	AMD_Win_J917_1dyn
AMD	Opteron 62xx	Windows Server 2008 R2 SP1	J9 1.7.0 SR1	AMD_Win_J917_1dyn
AMD	Opteron 62xx	Windows Server 2008 R2 SP1	J9 1.7.0 SR2	AMD_Win_J917_1dyn
AMD	Opteron 63xx	Windows Server 2008 R2 SP1	J9 1.7.0 SR1	AMD_Win_J917_1dyn
AMD	Opteron 63xx	Windows Server 2008 R2 SP1	J9 1.7.0 SR2	AMD_Win_J917_1dyn
AMD	Opteron 32xx	Windows Server 2012 R2	J9 1.7.0 SR1	AMD_Win_J917_2dyn
AMD	Opteron 32xx	Windows Server 2012 R2	J9 1.7.0 SR2	AMD_Win_J917_2dyn
AMD	Opteron 41xx	Windows Server 2012 R2	J9 1.7.0 SR1	AMD_Win_J917_2dyn
AMD	Opteron 41xx	Windows Server 2012 R2	J9 1.7.0 SR2	AMD_Win_J917_2dyn
AMD	Opteron 42xx	Windows Server 2012 R2	J9 1.7.0 SR1	AMD_Win_J917_2dyn
AMD	Opteron 42xx	Windows Server 2012 R2	J9 1.7.0 SR2	AMD_Win_J917_2dyn
AMD	Opteron 43xx	Windows Server 2012 R2	J9 1.7.0 SR1	AMD_Win_J917_2dyn
AMD	Opteron 43xx	Windows Server 2012 R2	J9 1.7.0 SR2	AMD_Win_J917_2dyn
AMD	Opteron 61xx	Windows Server 2012 R2	J9 1.7.0 SR1	AMD_Win_J917_2dyn
AMD	Opteron 61xx	Windows Server 2012 R2	J9 1.7.0 SR2	AMD_Win_J917_2dyn
AMD	Opteron 62xx	Windows Server 2012 R2	J9 1.7.0 SR1	AMD_Win_J917_2dyn
AMD	Opteron 62xx	Windows Server 2012 R2	J9 1.7.0 SR2	AMD_Win_J917_2dyn

AMD	Opteron 63xx	Windows Server 2012 R2	J9 1.7.0 SR1	AMD_Win_J917_2dyn
AMD	Opteron 63xx	Windows Server 2012 R2	J9 1.7.0 SR2	AMD_Win_J917_2dyn
AMD	Opteron 32xx	Red Hat Enterprise Linux Server 6	J9 1.7.0 SR1	AMD_Lin_J917_1dyn
AMD	Opteron 32xx	Red Hat Enterprise Linux Server 6	J9 1.7.0 SR2	AMD_Lin_J917_1dyn
AMD	Opteron 32xx	SUSE Linux Enterprise Server 11	J9 1.7.0 SR1	AMD_Lin_J917_1dyn
AMD	Opteron 32xx	SUSE Linux Enterprise Server 11	J9 1.7.0 SR2	AMD_Lin_J917_1dyn
AMD	Opteron 32xx	Oracle Linux 6	J9 1.7.0 SR1	AMD_Lin_J917_1dyn
AMD	Opteron 32xx	Oracle Linux 6	J9 1.7.0 SR2	AMD_Lin_J917_1dyn
AMD	Opteron 41xx	Red Hat Enterprise Linux Server 6	J9 1.7.0 SR1	AMD_Lin_J917_1dyn
AMD	Opteron 41xx	Red Hat Enterprise Linux Server 6	J9 1.7.0 SR2	AMD_Lin_J917_1dyn
AMD	Opteron 41xx	SUSE Linux Enterprise Server 11	J9 1.7.0 SR1	AMD_Lin_J917_1dyn
AMD	Opteron 41xx	SUSE Linux Enterprise Server 11	J9 1.7.0 SR2	AMD_Lin_J917_1dyn
AMD	Opteron 41xx	Oracle Linux 6	J9 1.7.0 SR1	AMD_Lin_J917_1dyn
AMD	Opteron 41xx	Oracle Linux 6	J9 1.7.0 SR2	AMD_Lin_J917_1dyn
AMD	Opteron 42xx	Red Hat Enterprise Linux Server 6	J9 1.7.0 SR1	AMD_Lin_J917_1dyn
AMD	Opteron 42xx	Red Hat Enterprise Linux Server 6	J9 1.7.0 SR2	AMD_Lin_J917_1dyn
AMD	Opteron 42xx	SUSE Linux Enterprise Server 11	J9 1.7.0 SR1	AMD_Lin_J917_1dyn
AMD	Opteron 42xx	SUSE Linux Enterprise Server 11	J9 1.7.0 SR2	AMD_Lin_J917_1dyn
AMD	Opteron 42xx	Oracle Linux 6	J9 1.7.0 SR1	AMD_Lin_J917_1dyn
AMD	Opteron 42xx	Oracle Linux 6	J9 1.7.0 SR2	AMD_Lin_J917_1dyn
AMD	Opteron 43xx	Red Hat Enterprise Linux Server 6	J9 1.7.0 SR1	AMD_Lin_J917_1dyn
AMD	Opteron 43xx	Red Hat Enterprise Linux Server 6	J9 1.7.0 SR2	AMD_Lin_J917_1dyn
AMD	Opteron 43xx	SUSE Linux Enterprise Server 11	J9 1.7.0 SR1	AMD_Lin_J917_1dyn
AMD	Opteron 43xx	SUSE Linux Enterprise Server 11	J9 1.7.0 SR2	AMD_Lin_J917_1dyn
AMD	Opteron 43xx	Oracle Linux 6	J9 1.7.0 SR1	AMD_Lin_J917_1dyn
AMD	Opteron 43xx	Oracle Linux 6	J9 1.7.0 SR2	AMD_Lin_J917_1dyn
AMD	Opteron 61xx	Red Hat Enterprise Linux Server 6	J9 1.7.0 SR1	AMD_Lin_J917_1dyn
AMD	Opteron 61xx	Red Hat Enterprise Linux Server 6	J9 1.7.0 SR2	AMD_Lin_J917_1dyn
AMD	Opteron 61xx	SUSE Linux Enterprise Server 11	J9 1.7.0 SR1	AMD_Lin_J917_1dyn
AMD	Opteron 61xx	SUSE Linux Enterprise Server 11	J9 1.7.0 SR2	AMD_Lin_J917_1dyn
AMD	Opteron 61xx	Oracle Linux 6	J9 1.7.0 SR1	AMD_Lin_J917_1dyn

AMD	Opteron 61xx	Oracle Linux 6	J9 1.7.0 SR2	AMD_Lin_J917_1dyn
AMD	Opteron 62xx	Red Hat Enterprise Linux Server 6	J9 1.7.0 SR1	AMD_Lin_J917_1dyn
AMD	Opteron 62xx	Red Hat Enterprise Linux Server 6	J9 1.7.0 SR2	AMD_Lin_J917_1dyn
AMD	Opteron 62xx	SUSE Linux Enterprise Server 11	J9 1.7.0 SR1	AMD_Lin_J917_1dyn
AMD	Opteron 62xx	SUSE Linux Enterprise Server 11	J9 1.7.0 SR2	AMD_Lin_J917_1dyn
AMD	Opteron 62xx	Oracle Linux 6	J9 1.7.0 SR1	AMD_Lin_J917_1dyn
AMD	Opteron 62xx	Oracle Linux 6	J9 1.7.0 SR2	AMD_Lin_J917_1dyn
AMD	Opteron 63xx	Red Hat Enterprise Linux Server 6	J9 1.7.0 SR1	AMD_Lin_J917_1dyn
AMD	Opteron 63xx	Red Hat Enterprise Linux Server 6	J9 1.7.0 SR2	AMD_Lin_J917_1dyn
AMD	Opteron 63xx	SUSE Linux Enterprise Server 11	J9 1.7.0 SR1	AMD_Lin_J917_1dyn
AMD	Opteron 63xx	SUSE Linux Enterprise Server 11	J9 1.7.0 SR2	AMD_Lin_J917_1dyn
AMD	Opteron 63xx	Oracle Linux 6	J9 1.7.0 SR1	AMD_Lin_J917_1dyn
AMD	Opteron 63xx	Oracle Linux 6	J9 1.7.0 SR2	AMD_Lin_J917_1dyn
AMD	Opteron A11xx	openSUSE Leap 42.x	OpenJDK 1.8.0	AMD_AArch64_Linux_OJDK18_1
IBM	POWER7	AIX 7.1	J9 1.7.0 SR1	IBM_AIX_J917_1dyn
IBM	POWER7	AIX 7.1	J9 1.7.0 SR2	IBM_AIX_J917_1dyn
IBM	POWER7+	AIX 7.1	J9 1.7.0 SR1	IBM_AIX_J917_1dyn
IBM	POWER7+	AIX 7.1	J9 1.7.0 SR2	IBM_AIX_J917_1dyn
IBM	POWER7	AIX 7.1	J9 1.7.0 SR3	IBM_AIX_J917_2dyn
IBM	POWER7	AIX 7.1	J9 1.7.0 SR6	IBM_AIX_J917_2dyn
IBM	POWER7+	AIX 7.1	J9 1.7.0 SR3	IBM_AIX_J917_2dyn
IBM	POWER7+	AIX 7.1	J9 1.7.0 SR6	IBM_AIX_J917_2dyn
IBM	POWER7	Red Hat Enterprise Linux Server 6	J9 1.7.0 SR3	IBM_Linux_J917_1dyn
IBM	POWER7	Red Hat Enterprise Linux Server 6	J9 1.7.0 SR6	IBM_Linux_J917_1dyn
IBM	POWER7+	Red Hat Enterprise Linux Server 6	J9 1.7.0 SR3	IBM_Linux_J917_1dyn
IBM	POWER7+	Red Hat Enterprise Linux Server 6	J9 1.7.0 SR6	IBM_Linux_J917_1dyn
IBM	POWER7	SUSE Linux Enterprise Server 11	J9 1.7.0 SR3	IBM_Linux_J917_2dyn
IBM	POWER7	SUSE Linux Enterprise Server 11	J9 1.7.0 SR6	IBM_Linux_J917_2dyn

IBM	POWER7+	SUSE Linux Enterprise Server 11	J9 1.7.0 SR3	IBM_Linux_J917_2dyn
IBM	POWER7+	SUSE Linux Enterprise Server 11	J9 1.7.0 SR6	IBM_Linux_J917_2dyn
IBM	POWER8	AIX 7.1	J9 v7r1	IBM_AIX_J971_1dyn
IBM	POWER8	AIX 7.1	J9 8.0 SR1	IBM_AIX_J980_1dyn
IBM	POWER8	AIX 7.1	J9 8.0 SR2	IBM_AIX_J980_1dyn
IBM	POWER8	AIX 7.1	J9 8.0 SR3+	IBM_AIX_J980_1dyn
IBM	POWER8	Red Hat Enterprise Linux Server 6	J9 v7r1	IBM_Linux_J971_1dyn
IBM	POWER8	Red Hat Enterprise Linux Server 7	J9 v7r1	IBM_Linux_J971_2dyn
IBM	POWER8	Red Hat Enterprise Linux Server 7	J9 8.0 SR1	IBM_Linux_J980_1dyn
IBM	POWER8	Red Hat Enterprise Linux Server 7	J9 8.0 SR2	IBM_Linux_J980_1dyn
IBM	POWER8	Red Hat Enterprise Linux Server 7	J9 8.0 SR3+	IBM_Linux_J980_1dyn
IBM	POWER8	Ubuntu 14.04.x	J9 8.0 SR1	IBM_Linux_J980_1dyn
IBM	POWER8	Ubuntu 14.04.x	J9 8.0 SR2	IBM_Linux_J980_1dyn
IBM	POWER8	Ubuntu 14.04.x	J9 8.0 SR3+	IBM_Linux_J980_1dyn
IBM	POWER8	Ubuntu 16.04.x	J9 8.0 SR3+	IBM_Linux_J980_1dyn
Oracle	SPARC T4	Solaris 11	HotSpot 1.7.0	SPARCT4_Sol_HS17_1
Fujitsu	SPARC64-X	Solaris 11	HotSpot 1.7.0	SPARC64_X_Sol_HS17_1

Annex B: Approved Hardware, Software and Power Analysers

The following list of power analysers and temperature sensors are approved for use with SEEM, and any restrictions to their use is noted. Additional power analysers can only be used with SEEM if they meet all the requirements of *Sub Clause 1.3.5*, and additional temperature sensors can only be used if they meet all the requirements of *Sub Clause 1.3.6*. Please note that not all power analysers or temperature sensors are compatible with all operating systems and data cable connection types. Please reference https://www.spec.org/power/docs/SPECpower-Device_Compatibility.html for more information.

Table 1 - Compliant Power Analysers

Manufacturer	Model	Restrictions on Use and Notes
Chroma	66202	Can only be used for low shunt ranges (0.01, 0.1, 0.4, 2.0 A RMS) and the 20A RMS high shunt range.
Chroma	66203, 66204	Only one channel at a time can be used.
Hioki	3334	With Hioki firmware version 1.10, the maximum valid load current must be less than 17.334A. For older firmware versions, only load currents less than 14.167A can be used.
Hioki	PW3335	Can only be used for load currents less than 20A
Hioki	PW3336	Single and multichannel Mode is supported. Can only be used with load currents less than 33.3A/channel
Hioki	PW3337	Single, multichannel and 3-phase mode is supported. Can only be used with load currents less than 33.3A/channel
Infratek	107A-1	Can only be used for load currents less than half the selected current range
Instek	GPM-8212	Can only be used for load currents less than 10A.
Newtons4th	PPA5x0	Can only be used for one channel at a time.
Newtons4th	PPA15x0	
Newtons4th	PPA55x0	Only Channel 1 can be used
Tektronix	PA1000	
Voltech	PM1000+	Firmware version 4.22 or newer is required
Xitron	2801	
Xitron	2802	Only one channel at a time can be used
Yokogawa	WT210	Firmware version 1.11 or newer is required. If installed, an external current sensor must be disabled.
Yokogawa	WT310, WT310e	Both 1-channel and 3-phase models can be used
Yokogawa	WT330, WT330e	Both 1-channel and 3-phase models can be used
Yokogawa	WT500	1-Channel, 3-Channel, and 3-Phase models can be used. For 1-Channel model, only the use of one channel at a time is

		supported. For 3-phase model, use of the summation feature for 3-channels is required.
Yokogawa	WT1800	Only one channel at a time can be used. If installed, an external current sensor must be disabled.
ZES Zimmer	LMG95	
ZES Zimmer	LMG450	1-Channel, 4-Channel, and 3-Phase models can be used. For 1-Channel model, only the use of one channel at a time is supported. For 3-phase model, use of the summation feature for 3-channels is required.
ZES Zimmer	LMG500	1-Channel, 4-Channel, and 3-Phase models can be used. For 1-Channel model, only the use of one channel at a time is supported. For 3-phase model, use of the summation feature for 3-channels is required.

Table 2 - Compliant Temperature Sensors

Manufacturer	Model
Digi	Watchport/H
Digi	Watchport/T
Temperature@lert	TM-STD30
iButtonLink	LinkUSBi + T-Sense®
iButtonLink	LinkUSBi + T-Probe