



SPEC® CINT2006 Result

Copyright 2006-2018 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6130, 2.10 GHz)

SPECint®_rate2006 = 3290

SPECint_rate_base2006 = 3120

CPU2006 license: 9019

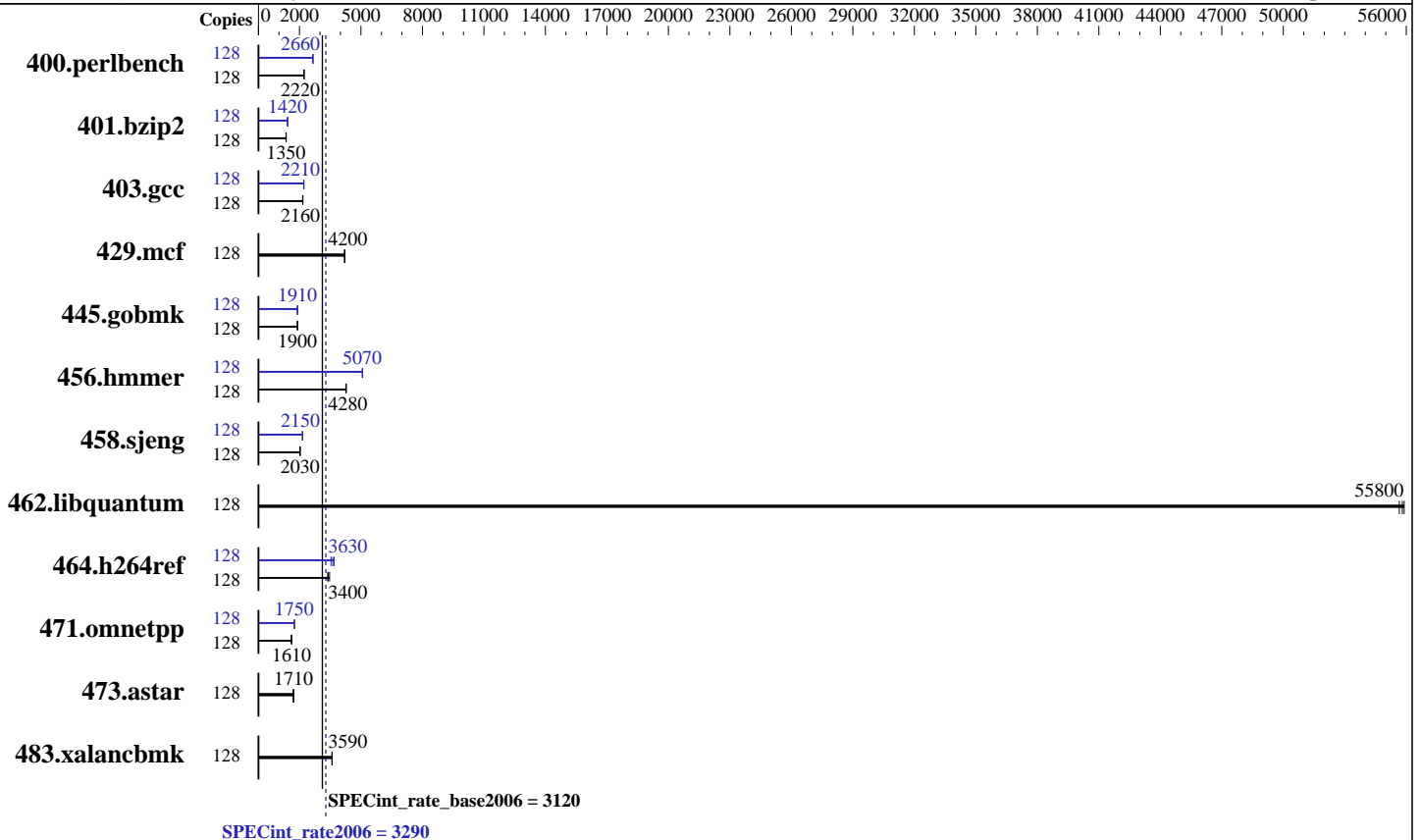
Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Dec-2009

Hardware Availability: Aug-2017

Software Availability: Sep-2017



Hardware

CPU Name: Intel Xeon Gold 6130
 CPU Characteristics: Intel Turbo Boost Technology up to 3.70 GHz
 CPU MHz: 2100
 FPU: Integrated
 CPU(s) enabled: 64 cores, 4 chips, 16 cores/chip, 2 threads/core
 CPU(s) orderable: 2,4 chips
 Primary Cache: 32 KB I + 32 KB D on chip per core
 Secondary Cache: 1 MB I+D on chip per core
 L3 Cache: 22 MB I+D on chip per chip
 Other Cache: None
 Memory: 768 GB (48 x 16 GB 2Rx4 PC4-2666V-R)
 Disk Subsystem: 1 x 600 GB SAS HDD, 10K RPM
 Other Hardware: None

Software

Operating System: SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.21-69-default
 Compiler: C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux;
 Fortran: Version 18.0.0.128 of Intel Fortran
 Auto Parallel: Yes
 File System: xfs
 System State: Run level 3 (multi-user)
 Base Pointers: 32-bit
 Peak Pointers: 32/64-bit
 Other Software: Microquill SmartHeap V10.2



SPEC CINT2006 Result

Copyright 2006-2018 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6130, 2.10 GHz)

SPECint_rate2006 = 3290

SPECint_rate_base2006 = 3120

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Dec-2009
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
400.perlbench	128	563	2220	561	2230	563	2220	128	471	2660	471	2660	471	2660
401.bzip2	128	914	1350	918	1340	915	1350	128	867	1420	873	1410	869	1420
403.gcc	128	478	2160	476	2160	476	2170	128	465	2220	465	2210	467	2210
429.mcf	128	278	4200	278	4200	277	4220	128	278	4200	278	4200	277	4220
445.gobmk	128	708	1900	707	1900	705	1910	128	703	1910	705	1910	707	1900
456.hammer	128	279	4280	279	4270	279	4280	128	235	5070	236	5070	235	5080
458.sjeng	128	763	2030	762	2030	764	2030	128	720	2150	721	2150	722	2150
462.libquantum	128	47.6	55700	47.5	55800	47.4	55900	128	47.6	55700	47.5	55800	47.4	55900
464.h264ref	128	834	3400	837	3380	816	3470	128	767	3690	781	3630	801	3540
471.omnetpp	128	496	1610	495	1620	497	1610	128	457	1750	456	1760	457	1750
473.astar	128	525	1710	526	1710	527	1710	128	525	1710	526	1710	527	1710
483.xalancbmk	128	245	3600	247	3580	246	3590	128	245	3600	247	3580	246	3590

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes

BIOS Settings:

Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6993
Revision 6993 of 2015-11-06 (b5e8d4b4eb51ed28d7f98696cbe290c1)
running on linux-vb5q Thu Dec 31 20:03:55 2009

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
<http://www.spec.org/cpu2006/Docs/config.html#sysinfo>

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6130 CPU @ 2.10GHz
Continued on next page



SPEC CINT2006 Result

Copyright 2006-2018 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6130, 2.10 GHz)

SPECint_rate2006 = 3290

SPECint_rate_base2006 = 3120

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Dec-2009
Hardware Availability: Aug-2017
Software Availability: Sep-2017

Platform Notes (Continued)

```

4 "physical id"s (chips)
128 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The
following excerpts from /proc/cpuinfo might not be reliable. Use with
caution.)
cpu cores : 16
siblings  : 32
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
physical 2: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
physical 3: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
cache size : 22528 KB

```

```

From /proc/meminfo
MemTotal:      791027716 kB
HugePages_Total:      0
Hugepagesize:    2048 kB

```

```

From /etc/*release* /etc/*version*
SuSE-release:
SUSE Linux Enterprise Server 12 (x86_64)
VERSION = 12
PATCHLEVEL = 2
# This file is deprecated and will be removed in a future service pack or
release.
# Please check /etc/os-release for details about this release.
os-release:
NAME="SLES"
VERSION="12-SP2"
VERSION_ID="12.2"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp2"

```

```

uname -a:
Linux linux-vb5q 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016
(9464f67) x86_64 x86_64 x86_64 GNU/Linux

```

run-level 3 Dec 31 19:19

```

SPEC is set to: /opt/cpu2006-1.2
Filesystem      Type  Size  Used Avail Use% Mounted on
/dev/sdal        xfs   280G  118G  162G  43% /
Additional information from dmidecode:

```

Warning: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B480M5.3.2.2a.0.0919171641 09/19/2017
Continued on next page



SPEC CINT2006 Result

Copyright 2006-2018 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6130, 2.10 GHz)

SPECint_rate2006 = 3290

SPECint_rate_base2006 = 3120

CPU2006 license: 9019

Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Dec-2009

Hardware Availability: Aug-2017

Software Availability: Sep-2017

Platform Notes (Continued)

Memory:

48x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666 MHz

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:

`LD_LIBRARY_PATH = */opt/intel/compilers_and_libraries_2018.0.128/linux/compiler/lib/ia32:/opt/intel/compilers_and_libraries_2018.0.128/linux/compiler/lib/intel64:/opt/cpu2006-1.2/sh10.2*`

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM

memory using Redhat Enterprise Linux 7.2

Transparent Huge Pages enabled with:

`echo always > /sys/kernel/mm/transparent_hugepage/enabled`

Filesystem page cache cleared with:

shell invocation of `'sync; echo 3 > /proc/sys/vm/drop_caches'` prior to run

runspec command invoked through numactl i.e.:

`numactl --interleave=all runspec <etc>`

No: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

No: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

No: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

This benchmark result is intended to provide perspective on past performance using the historical hardware and/or software described on this result page.

The system as described on this result page was formerly generally available. At the time of this publication, it may not be shipping, and/or may not be supported, and/or may fail to meet other tests of General Availability described in the SPEC OSG Policy document, <http://www.spec.org/osg/policy.html>

This measured result may not be representative of the result that would be measured were this benchmark run with hardware and software available as of the publication date.

Base Compiler Invocation

C benchmarks:

`icc -m32 -L/opt/intel/compilers_and_libraries_2018.0.128/linux/lib/ia32`

C++ benchmarks:

`icpc -m32 -L/opt/intel/compilers_and_libraries_2018.0.128/linux/lib/ia32`



SPEC CINT2006 Result

Copyright 2006-2018 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6130, 2.10 GHz)

SPECint_rate2006 = 3290

SPECint_rate_base2006 = 3120

CPU2006 license: 9019

Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Dec-2009

Hardware Availability: Aug-2017

Software Availability: Sep-2017

Base Portability Flags

```

400.perlbench: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX_IA32
401.bzip2: -D_FILE_OFFSET_BITS=64
403.gcc: -D_FILE_OFFSET_BITS=64
429.mcf: -D_FILE_OFFSET_BITS=64
445.gobmk: -D_FILE_OFFSET_BITS=64
456.hmmer: -D_FILE_OFFSET_BITS=64
458.sjeng: -D_FILE_OFFSET_BITS=64
462.libquantum: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
464.h264ref: -D_FILE_OFFSET_BITS=64
471.omnetpp: -D_FILE_OFFSET_BITS=64
473.astar: -D_FILE_OFFSET_BITS=64
483.xalancbmk: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX

```

Base Optimization Flags

C benchmarks:

-xHOST -ipo -O3 -no-prec-div -qopt-prefetch -qopt-mem-layout-trans=3

C++ benchmarks:

-xHOST -ipo -O3 -no-prec-div -qopt-prefetch -qopt-mem-layout-trans=3
-Wl,-z,muldefs -L/opt/cpu2006-1.2/sh10.2 -lsmarthearp

Base Other Flags

C benchmarks:

403.gcc: -Dalloca=_alloca

Peak Compiler Invocation

C benchmarks (except as noted below):

icc -m32 -L/opt/intel/compilers_and_libraries_2018.0.128/linux/lib/ia32

400.perlbench: icc -m64

401.bzip2: icc -m64

456.hmmer: icc -m64

458.sjeng: icc -m64

C++ benchmarks:

icpc -m32 -L/opt/intel/compilers_and_libraries_2018.0.128/linux/lib/ia32



SPEC CINT2006 Result

Copyright 2006-2018 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6130, 2.10 GHz)

SPECint_rate2006 = 3290

SPECint_rate_base2006 = 3120

CPU2006 license: 9019

Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Dec-2009

Hardware Availability: Aug-2017

Software Availability: Sep-2017

Peak Portability Flags

```

400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64
401.bzip2: -DSPEC_CPU_LP64
403.gcc: -D_FILE_OFFSET_BITS=64
429.mcf: -D_FILE_OFFSET_BITS=64
445.gobmk: -D_FILE_OFFSET_BITS=64
456.hmmer: -DSPEC_CPU_LP64
458.sjeng: -DSPEC_CPU_LP64
462.libquantum: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
464.h264ref: -D_FILE_OFFSET_BITS=64
471.omnetpp: -D_FILE_OFFSET_BITS=64
473.astar: -D_FILE_OFFSET_BITS=64
483.xalancbmk: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX

```

Peak Optimization Flags

C benchmarks:

```

400.perlbench: -prof-gen(pass 1) -prof-use(pass 2) -xHOST(pass 2)
               -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
               -no-prec-div(pass 2) -auto-ilp32 -qopt-mem-layout-trans=3

401.bzip2: -prof-gen(pass 1) -prof-use(pass 2) -xHOST(pass 2)
            -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
            -no-prec-div(pass 2) -qopt-prefetch -auto-ilp32
            -qopt-mem-layout-trans=3

403.gcc: -xHOST -ipo -O3 -no-prec-div -qopt-mem-layout-trans=3

429.mcf: basepeak = yes

445.gobmk: -prof-gen(pass 1) -prof-use(pass 2) -xHOST(pass 2)
            -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
            -no-prec-div(pass 2) -qopt-mem-layout-trans=3

456.hmmer: -xHOST -ipo -O3 -no-prec-div -unroll2 -auto-ilp32
            -qopt-mem-layout-trans=3

458.sjeng: -prof-gen(pass 1) -prof-use(pass 2) -xHOST(pass 2)
            -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
            -no-prec-div(pass 2) -unroll14 -auto-ilp32
            -qopt-mem-layout-trans=3

462.libquantum: basepeak = yes

464.h264ref: -prof-gen(pass 1) -prof-use(pass 2) -xHOST(pass 2)
              -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
              -no-prec-div(pass 2) -unroll2 -qopt-mem-layout-trans=3

```

Continued on next page



SPEC CINT2006 Result

Copyright 2006-2018 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6130, 2.10 GHz)

SPECint_rate2006 = 3290

SPECint_rate_base2006 = 3120

CPU2006 license: 9019

Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Dec-2009

Hardware Availability: Aug-2017

Software Availability: Sep-2017

Peak Optimization Flags (Continued)

C++ benchmarks:

```
471.omnetpp: -prof-gen(pass 1) -prof-use(pass 2) -xHOST(pass 2)
             -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
             -no-prec-div(pass 2)
             -qopt-ra-region-strategy=block
             -qopt-mem-layout-trans=3 -Wl,-z,muldefs
             -L/opt/cpu2006-1.2/sh10.2 -lsmartheap
```

473.astar: basepeak = yes

483.xalancbmk: basepeak = yes

Peak Other Flags

C benchmarks:

```
403.gcc: -Dalloca=_alloca
```

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.html>
<http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.xml>
<http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.xml>

SPEC and SPECint are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.2.
Report generated on Fri Apr 20 19:48:04 2018 by SPEC CPU2006 PS/PDF formatter v6932.
Originally published on 23 February 2018.