



SPEC® CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M3 (Intel Xeon E5-2650 v2 @ 2.60 GHz)

SPECint_rate2006 = 689

SPECint_rate_base2006 = 662

CPU2006 license: 9019

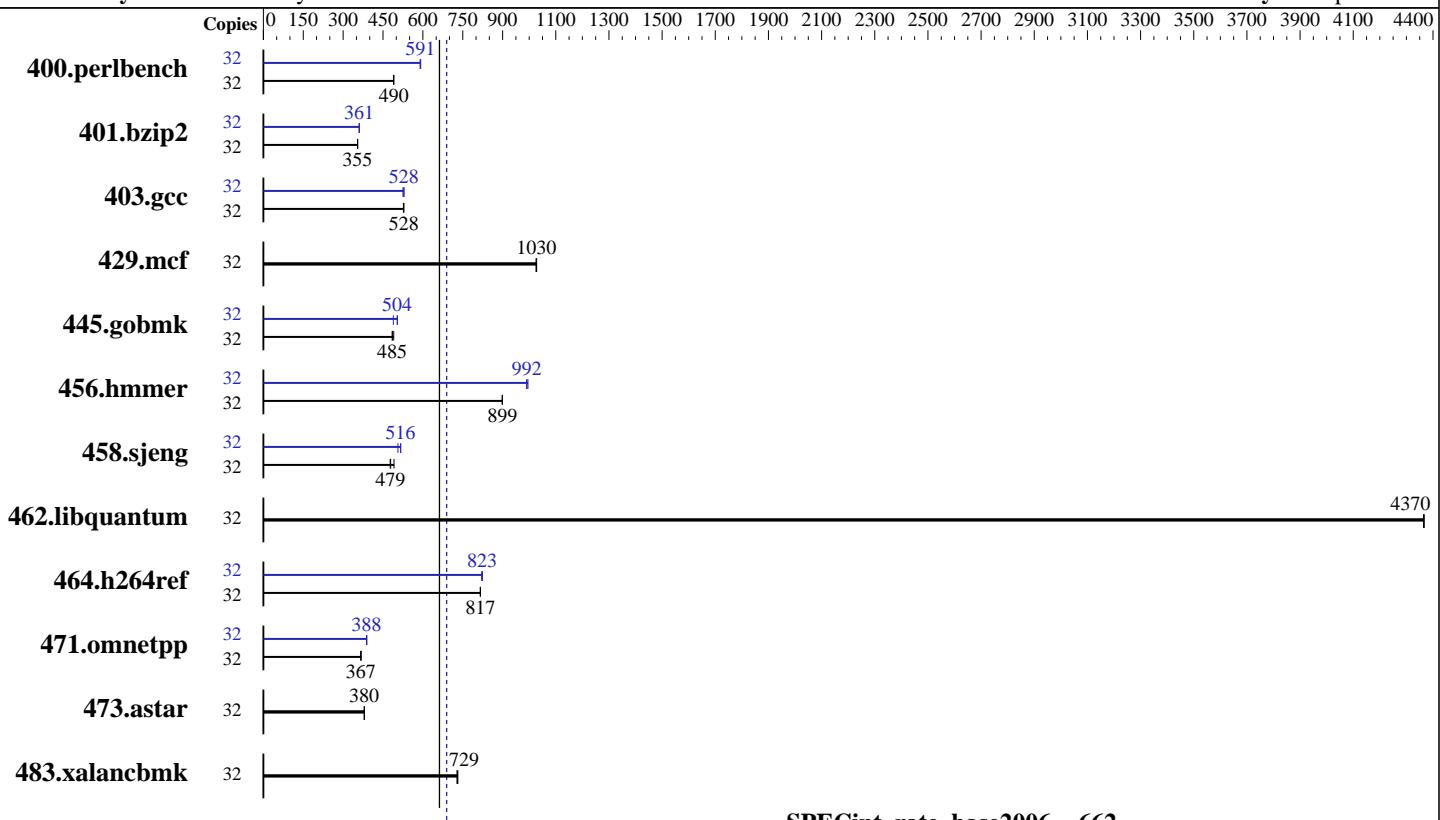
Test date: Oct-2013

Test sponsor: Cisco Systems

Hardware Availability: Sep-2013

Tested by: Cisco Systems

Software Availability: Sep-2013



SPECint_rate_base2006 = 662

SPECint_rate2006 = 689

Hardware

CPU Name:	Intel Xeon E5-2650 v2
CPU Characteristics:	Intel Turbo Boost Technology up to 3.40 GHz
CPU MHz:	2600
FPU:	Integrated
CPU(s) enabled:	16 cores, 2 chips, 8 cores/chip, 2 threads/core
CPU(s) orderable:	1,2 chips
Primary Cache:	32 KB I + 32 KB D on chip per core
Secondary Cache:	256 KB I+D on chip per core
L3 Cache:	20 MB I+D on chip per chip
Other Cache:	None
Memory:	128 GB (16 x 8 GB 2Rx4 PC3-14900R-11, ECC)
Disk Subsystem:	1 X 600GB SAS, 15K RPM
Other Hardware:	None

Software

Operating System:	Red Hat Enterprise Linux Server release 6.4 (Santiago) 2.6.32-358.el6.x86_64
Compiler:	C/C++: Version 14.0.0.080 of Intel C++ Studio XE for Linux
Auto Parallel:	No
File System:	ext4
System State:	Run level 3 (multi-user)
Base Pointers:	32-bit
Peak Pointers:	32/64-bit
Other Software:	Microquill SmartHeap V10.0



SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M3 (Intel Xeon E5-2650 v2 @ 2.60 GHz)

SPECint_rate2006 = 689

SPECint_rate_base2006 = 662

CPU2006 license: 9019

Test date: Oct-2013

Test sponsor: Cisco Systems

Hardware Availability: Sep-2013

Tested by: Cisco Systems

Software Availability: Sep-2013

Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
400.perlbench	32	638	490	637	490	638	490	32	529	591	530	590	528	592
401.bzip2	32	872	354	871	355	871	355	32	856	361	854	361	857	360
403.gcc	32	489	527	488	528	488	528	32	491	525	488	528	487	529
429.mcf	32	285	1030	284	1030	284	1030	32	285	1030	284	1030	284	1030
445.gobmk	32	692	485	685	490	692	485	32	687	489	666	504	666	504
456.hammer	32	332	898	332	899	332	899	32	301	992	300	995	301	990
458.sjeng	32	809	479	788	491	812	477	32	765	506	750	516	750	517
462.libquantum	32	152	4360	152	4370	152	4370	32	152	4360	152	4370	152	4370
464.h264ref	32	867	817	867	817	868	816	32	859	824	860	823	862	821
471.omnetpp	32	546	367	546	366	544	368	32	515	388	515	388	514	389
473.astar	32	592	379	591	380	592	380	32	592	379	591	380	592	380
483.xalancbmk	32	303	729	303	729	302	732	32	303	729	303	729	302	732

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes

BIOS Settings:

Intel HT Technology = Enabled

CPU performance set to HPC

Power Technology set to Custom

CPU Power State C6 set to Enabled

CPU Power State C1 Enhanced set to Disabled

Energy Performance policy set to Performance

Memory RAS configuration set to Maximum Performance

DRAM Clock Throttling Set to Performance

LV DDR Mode set to Performance-mode

DRAM Refresh Rate Set to 1x

Intel HT Technology = Enable

Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6818

\$Rev: 6818 \$ \$Date::: 2012-07-17 ## e86d102572650a6e4d596a3cee98f191

running on localhost.localdomain Thu Oct 3 20:53:36 2013

This section contains SUT (System Under Test) info as seen by

Continued on next page



SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M3 (Intel Xeon E5-2650 v2 @ 2.60 GHz)

SPECint_rate2006 = 689

SPECint_rate_base2006 = 662

CPU2006 license: 9019

Test date: Oct-2013

Test sponsor: Cisco Systems

Hardware Availability: Sep-2013

Tested by: Cisco Systems

Software Availability: Sep-2013

Platform Notes (Continued)

some common utilities. To remove or add to this section, see:
<http://www.spec.org/cpu2006/Docs/config.html#sysinfo>

```
From /proc/cpuinfo
    model name : Intel(R) Xeon(R) CPU E5-2650 v2 @ 2.60GHz
        2 "physical id"s (chips)
            32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The
following excerpts from /proc/cpuinfo might not be reliable. Use with
caution.)
    cpu cores : 8
    siblings   : 16
    physical 0: cores 0 1 2 3 4 5 6 7
    physical 1: cores 0 1 2 3 4 5 6 7
cache size : 20480 KB
```

```
From /proc/meminfo
MemTotal:      132087400 kB
HugePages_Total:       0
Hugepagesize:     2048 kB
```

```
/usr/bin/lsb_release -d
Red Hat Enterprise Linux Server release 6.4 (Santiago)
```

```
From /etc/*release* /etc/*version*
redhat-release: Red Hat Enterprise Linux Server release 6.4 (Santiago)
system-release: Red Hat Enterprise Linux Server release 6.4 (Santiago)
system-release-cpe: cpe:/o:redhat:enterprise_linux:6server:ga:server
```

```
uname -a:
Linux localhost.localdomain 2.6.32-358.el6.x86_64 #1 SMP Tue Jan 29 11:47:41
EST 2013 x86_64 x86_64 x86_64 GNU/Linux
```

```
run-level 3 Oct 3 20:52
```

```
SPEC is set to: /opt/cpu2006-1.2
Filesystem      Type  Size  Used Avail Use% Mounted on
/dev/sdal      ext4   550G   17G  505G   4%  /
```

Additional information from dmidecode:

```
BIOS Cisco Systems, Inc. B200M3.2.1.3a.0.082320131800 08/23/2013
Memory:
16x 0xAD00 HMT31GR7EFR4C-RD 8 GB 1866 MHz 2 rank
8x NO DIMM NO DIMM
```

(End of data from sysinfo program)



SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M3 (Intel Xeon E5-2650 v2 @ 2.60 GHz)

SPECint_rate2006 = 689

SPECint_rate_base2006 = 662

CPU2006 license: 9019

Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Oct-2013

Hardware Availability: Sep-2013

Software Availability: Sep-2013

General Notes

Environment variables set by runspec before the start of the run:

LD_LIBRARY_PATH = "/opt/cpu2006-1.2/libs/32:/opt/cpu2006-1.2/libs/64:/opt/cpu2006-1.2/sh"

Binaries compiled on a system with 1x Core i7-860 CPU + 8GB

memory using RedHat EL 6.4

Transparent Huge Pages enabled with:

echo always > /sys/kernel/mm/redhat_transparent_hugepage/enabled

Filesystem page cache cleared with:

echo 1> /proc/sys/vm/drop_caches

runspec command invoked through numactl i.e.:

numactl --interleave=all runspec <etc>

Base Compiler Invocation

C benchmarks:

icc -m32

C++ benchmarks:

icpc -m32

Base Portability Flags

400.perlbench: -DSPEC_CPU_LINUX_IA32

462.libquantum: -DSPEC_CPU_LINUX

483.xalancbmk: -DSPEC_CPU_LINUX

Base Optimization Flags

C benchmarks:

-xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -opt-mem-layout-trans=3

C++ benchmarks:

-xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -opt-mem-layout-trans=3
-Wl,-z,muldefs -L/sh -lsmartheap

Base Other Flags

C benchmarks:

403.gcc: -Dalloca=_alloca



SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M3 (Intel Xeon E5-2650 v2 @ 2.60 GHz)

SPECint_rate2006 = 689

SPECint_rate_base2006 = 662

CPU2006 license: 9019

Test date: Oct-2013

Test sponsor: Cisco Systems

Hardware Availability: Sep-2013

Tested by: Cisco Systems

Software Availability: Sep-2013

Peak Compiler Invocation

C benchmarks (except as noted below):

icc -m32

400.perlbench: icc -m64

401.bzip2: icc -m64

456.hmmer: icc -m64

458.sjeng: icc -m64

C++ benchmarks:

icpc -m32

Peak Portability Flags

400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64

401.bzip2: -DSPEC_CPU_LP64

456.hmmer: -DSPEC_CPU_LP64

458.sjeng: -DSPEC_CPU_LP64

462.libquantum: -DSPEC_CPU_LINUX

483.xalancbmk: -DSPEC_CPU_LINUX

Peak Optimization Flags

C benchmarks:

400.perlbench: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-auto-ilp32

401.bzip2: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-opt-prefetch -auto-ilp32 -ansi-alias

403.gcc: -xSSE4.2 -ipo -O3 -no-prec-div

429.mcf: basepeak = yes

445.gobmk: -xSSE4.2(pass 2) -prof-gen(pass 1) -prof-use(pass 2)
-ansi-alias -opt-mem-layout-trans=3

456.hmmer: -xSSE4.2 -ipo -O3 -no-prec-div -unroll12 -auto-ilp32

458.sjeng: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-unroll14 -auto-ilp32

Continued on next page



SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M3 (Intel Xeon E5-2650 v2 @ 2.60 GHz)

SPECint_rate2006 = 689

SPECint_rate_base2006 = 662

CPU2006 license: 9019

Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Oct-2013

Hardware Availability: Sep-2013

Software Availability: Sep-2013

Peak Optimization Flags (Continued)

462.libquantum: basepeak = yes

```
464.h264ref: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
              -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
              -unroll12 -ansi-alias
```

C++ benchmarks:

```
471.omnetpp: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
              -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
              -ansi-alias -opt-ra-region-strategy=block -Wl,-z,muldefs
              -L/sh -lsmartheap
```

473.astar: basepeak = yes

483.xalancbmk: basepeak = yes

Peak Other Flags

C benchmarks:

403.gcc: -Dalloca=__alloca

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.html>
<http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20130717.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.xml>
<http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20130717.xml>

SPEC and SPECint are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.2.

Report generated on Thu Jul 24 19:15:54 2014 by SPEC CPU2006 PS/PDF formatter v6932.

Originally published on 5 November 2013.