SPEC® CINT2006 Result

IBM Corporation

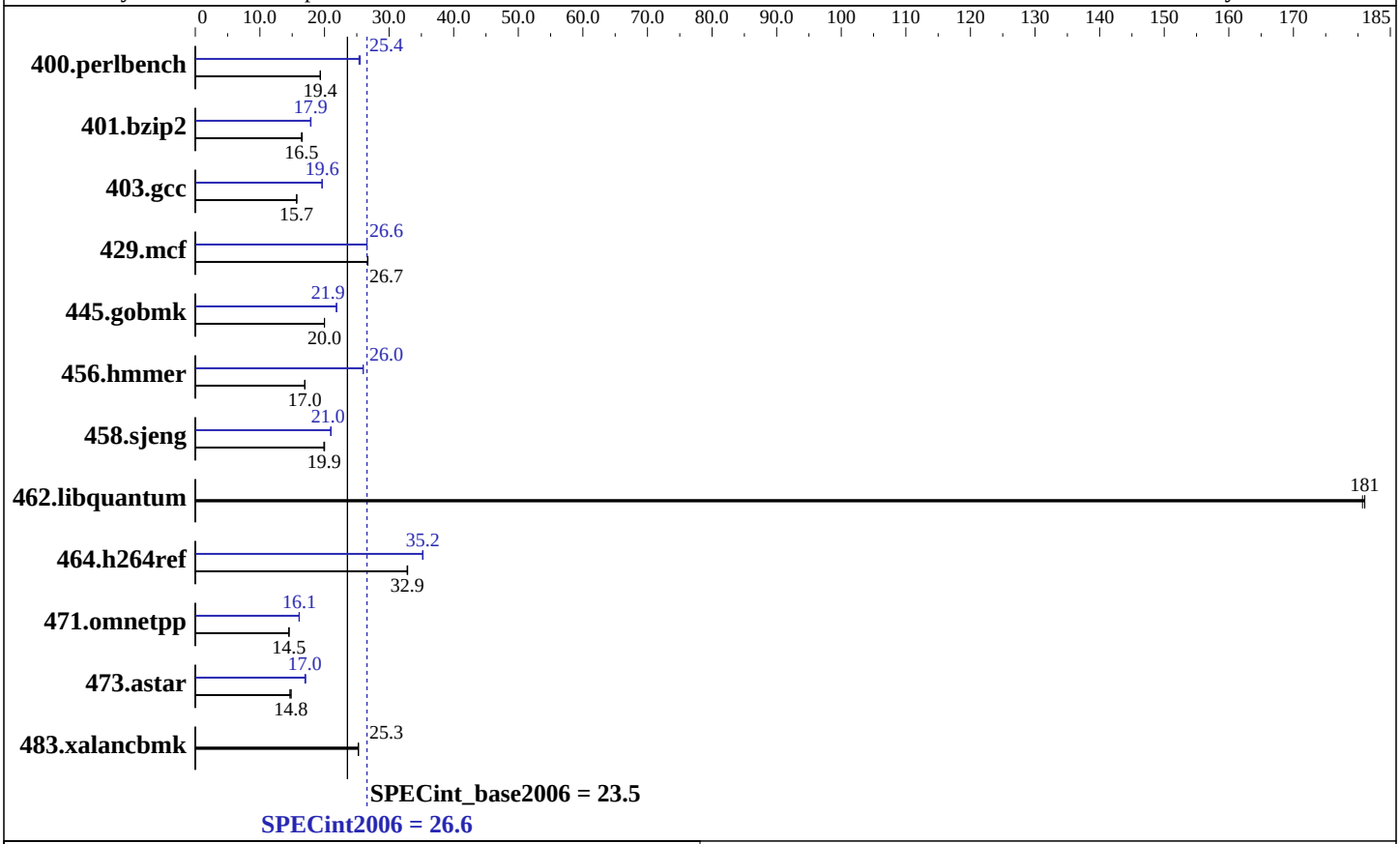
IBM System x iDataPlex dx360 (Intel Xeon L5240)

SPECint®2006 = 26.6

SPECint_base2006 = 23.5

CPU2006 license: 11
Test sponsor: IBM Corporation
Tested by: IBM Corporation

Test date: Mar-2009
Hardware Availability: Nov-2008
Software Availability: Feb-2009



Hardware

CPU Name:	Intel Xeon L5240
CPU Characteristics:	1333MHz system bus
CPU MHz:	3000
FPU:	Integrated
CPU(s) enabled:	4 cores, 2 chips, 2 cores/chip
CPU(s) orderable:	1,2 chips
Primary Cache:	32 KB I + 32 KB D on chip per core
Secondary Cache:	6 MB I+D on chip per chip
L3 Cache:	None
Other Cache:	None
Memory:	16 GB (8 x 2 GB DDR2-5300F ECC)
Disk Subsystem:	1 x 250 GB SATA, 7200 RPM
Other Hardware:	None

Software

Operating System:	SuSE Linux Enterprise Server 10(x86_64) SP2, Kernel 2.6.16.60-0.21-smp
Compiler:	Intel C++ Compiler 11.0 for Linux Build 20080930 Package ID: l_cproc_p_11.0.066
Auto Parallel:	Yes
File System:	ReiserFS
System State:	Run level 3 (multi-user)
Base Pointers:	32-bit
Peak Pointers:	32/64-bit
Other Software:	Microquill SmartHeap V8.1 Binutils 2.18.50.0.7.20080502

SPEC CINT2006 Result

IBM Corporation

IBM System x iDataPlex dx360 (Intel Xeon L5240)

SPECint2006 = 26.6

SPECint_base2006 = 23.5

CPU2006 license: 11
Test sponsor: IBM Corporation
Tested by: IBM Corporation

Test date: Mar-2009
Hardware Availability: Nov-2008
Software Availability: Feb-2009

Results Table

Benchmark	Base						Peak					
	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
400.perlbench	505	19.3	504	19.4	**505**	**19.4**	386	25.3	383	25.5	**384**	**25.4**
401.bzip2	583	16.6	586	16.5	**586**	**16.5**	**540**	**17.9**	541	17.8	539	17.9
403.gcc	511	15.7	**514**	**15.7**	515	15.6	**410**	**19.6**	410	19.6	410	19.6
429.mcf	342	26.7	**341**	**26.7**	341	26.7	343	26.6	**343**	**26.6**	343	26.6
445.gobmk	525	20.0	**525**	**20.0**	525	20.0	**480**	**21.9**	480	21.9	480	21.9
456.hmmer	**550**	**17.0**	550	17.0	550	17.0	359	26.0	**359**	**26.0**	359	26.0
458.sjeng	604	20.0	**607**	**19.9**	607	19.9	575	21.0	**577**	**21.0**	577	21.0
462.libquantum	114	181	**114**	**181**	115	181	114	181	**114**	**181**	115	181
464.h264ref	**674**	**32.9**	673	32.9	675	32.8	628	35.3	**628**	**35.2**	629	35.2
471.omnetpp	431	14.5	**431**	**14.5**	431	14.5	388	16.1	**388**	**16.1**	389	16.1
473.astar	**474**	**14.8**	479	14.6	474	14.8	**413**	**17.0**	413	17.0	410	17.1
483.xalancbmk	273	25.3	**273**	**25.3**	274	25.2	273	25.3	**273**	**25.3**	274	25.2

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

General Notes

```
Hardware Sector Prefetch Enable and Adjacent Sector Prefetch Enable
OMP_NUM_THREADS set to number of processors
KMP_AFFINITY set to "physical,0"
```

Base Compiler Invocation

C benchmarks:
`icc`

C++ benchmarks:
`icpc`

Base Portability Flags

400.perlbench: `-DSPEC_CPU_LINUX_IA32`
462.libquantum: `-DSPEC_CPU_LINUX`
483.xalancbmk: `-DSPEC_CPU_LINUX`

Base Optimization Flags

C benchmarks:
`-xSSE4.1 -ipo -O3 -no-prec-div -static -parallel -par-runtime-control -opt-prefetch`

Continued on next page

Base Optimization Flags (Continued)

C++ benchmarks:
-xSSE4.1 -ipo -O3 -no-prec-div -opt-prefetch -Wl,-z,muldefs
-L/spec/cpu2006.1.1/lib -lsmartheap

Base Other Flags

C benchmarks:

403.gcc: -Dalloca=_alloca

Peak Compiler Invocation

C benchmarks (except as noted below):
icc

401.bzip2: /opt/intel/Compiler/11.0/066/bin/intel64/icc

456.hmmer: /opt/intel/Compiler/11.0/066/bin/intel64/icc

C++ benchmarks:
icpc

Peak Portability Flags

400.perlbench: -DSPEC_CPU_LINUX_IA32
401.bzip2: -DSPEC_CPU_LP64
456.hmmer: -DSPEC_CPU_LP64
462.libquantum: -DSPEC_CPU_LINUX
483.xalancbmk: -DSPEC_CPU_LINUX

Peak Optimization Flags

C benchmarks:

400.perlbench: -prof-gen(pass 1) -prof-use(pass 2) -xSSE4.1 -ipo -O3
-no-prec-div -static -ansi-alias -opt-prefetch

401.bzip2: -prof-gen(pass 1) -prof-use(pass 2) -xSSE4.1 -ipo -O3
-no-prec-div -static -auto-ilp32 -opt-prefetch
-ansi-alias

Continued on next page

Peak Optimization Flags (Continued)

403.gcc: `-xSSE4.1 -ipo -O3 -no-prec-div -static -inline-calloc -opt-malloc-options=3`

429.mcf: `-xSSE4.1 -ipo -O3 -no-prec-div -static -opt-prefetch`

445.gobmk: `-prof-gen`(pass 1) `-prof-use`(pass 2) `-xSSE4.1 -O2 -ipo -no-prec-div -ansi-alias`

456.hmmer: `-xSSE4.1 -ipo -O3 -no-prec-div -static -unroll2 -ansi-alias -auto-ilp32`

458.sjeng: `-prof-gen`(pass 1) `-prof-use`(pass 2) `-xSSE4.1 -ipo -O3 -no-prec-div -static -unroll4`

462.libquantum: `basepeak = yes`

464.h264ref: `-prof-gen`(pass 1) `-prof-use`(pass 2) `-xSSE4.1 -ipo -O3 -no-prec-div -static -unroll2 -ansi-alias`

C++ benchmarks:

471.omnetpp: `-prof-gen`(pass 1) `-prof-use`(pass 2) `-xSSE4.1 -ipo -O3 -no-prec-div -ansi-alias -opt-ra-region-strategy=block -Wl,-z,muldefs -L/spec/cpu2006.1.1/lib -lsmartheap`

473.astar: `-prof-gen`(pass 1) `-prof-use`(pass 2) `-xSSE4.1 -ipo -O3 -no-prec-div -ansi-alias -opt-ra-region-strategy=routine -Wl,-z,muldefs -L/spec/cpu2006.1.1/lib -lsmartheap`

483.xalancbmk: `basepeak = yes`

Peak Other Flags

C benchmarks:

403.gcc: `-Dalloca=_alloca`

The flags file that was used to format this result can be browsed at
`http://www.spec.org/cpu2006/flags/Intel-ic11.0-int-linux64-revA.20090710.17.html`

You can also download the XML flags source by saving the following link:
`http://www.spec.org/cpu2006/flags/Intel-ic11.0-int-linux64-revA.20090710.17.xml`

For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.1.
Report generated on Wed Jul 23 00:46:39 2014 by SPEC CPU2006 PS/PDF formatter v6932.
Originally published on 24 June 2009.