



# SPEC® CINT2006 Result

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## Hewlett-Packard Company

### SPECint®\_rate2006 = 156

ProLiant DL160 G5p  
(3.20 GHz, Intel Xeon X5482)

### SPECint\_rate\_base2006 = 145

CPU2006 license: 3

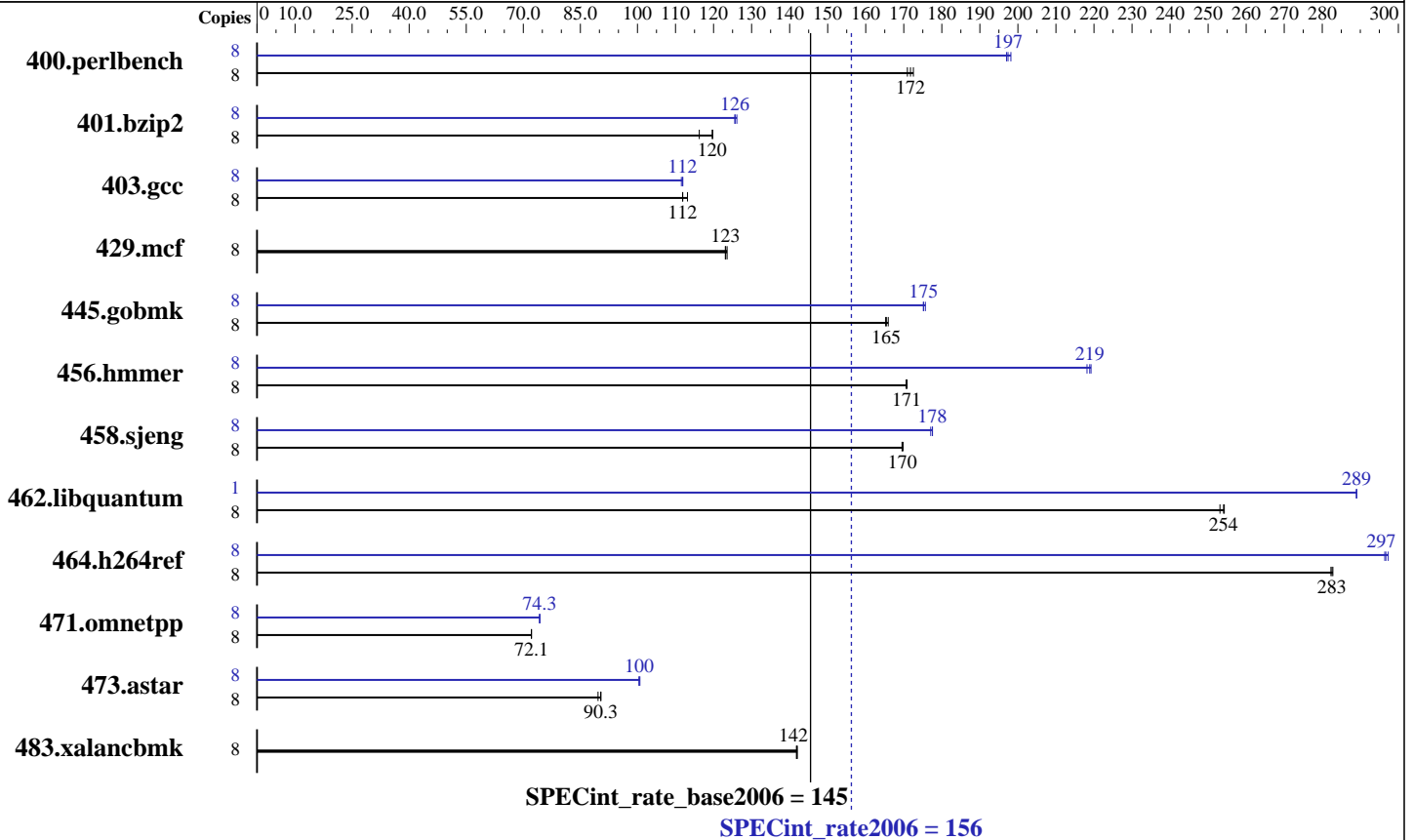
Test date: Aug-2008

Test sponsor: Hewlett-Packard Company

Hardware Availability: Sep-2008

Tested by: Hewlett-Packard Company

Software Availability: Nov-2008



### Hardware

CPU Name: Intel Xeon X5482  
 CPU Characteristics: 3.20 GHz, 2x6 MB L2 Shared, 1600 MHz system bus  
 CPU MHz: 3200  
 FPU: Integrated  
 CPU(s) enabled: 8 cores, 2 chips, 4 cores/chip  
 CPU(s) orderable: 1,2 chips  
 Primary Cache: 32 KB I + 32 KB D on chip per core  
 Secondary Cache: 12 MB I+D on chip per chip, 6 MB shared / 2 cores  
 L3 Cache: None  
 Other Cache: None  
 Memory: 16 GB (8x2 GB PC2-6400F CL5)  
 Disk Subsystem: 1x72 GB 15 K SAS  
 Other Hardware: None

### Software

Operating System: SUSE Linux Enterprise Server 10 (x86\_64) SP1, Kernel 2.6.16.46-0.12-smp  
 Compiler: Intel C++ Compiler 11.0 for Linux Build 20080730 Package ID: l\_cproc\_b\_11.0.042  
 Auto Parallel: Yes  
 File System: ext3  
 System State: Run level 3 (multi-user)  
 Base Pointers: 32-bit  
 Peak Pointers: 32/64-bit  
 Other Software: Microquill SmartHeap V8.1 Binutils 2.18.50.0.7.20080502



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## Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
400.perlbench	8	<b>455</b>	<b>172</b>	453	173	457	171	8	394	198	<b>396</b>	<b>197</b>	397	197
401.bzip2	8	664	116	644	120	<b>645</b>	<b>120</b>	8	615	126	612	126	<b>614</b>	<b>126</b>
403.gcc	8	569	113	<b>575</b>	<b>112</b>	576	112	8	<b>576</b>	<b>112</b>	575	112	577	112
429.mcf	8	593	123	<b>592</b>	<b>123</b>	590	124	8	593	123	<b>592</b>	<b>123</b>	590	124
445.gobmk	8	508	165	506	166	<b>507</b>	<b>165</b>	8	<b>479</b>	<b>175</b>	478	176	479	175
456.hammer	8	437	171	437	171	<b>437</b>	<b>171</b>	8	340	219	<b>341</b>	<b>219</b>	342	218
458.sjeng	8	571	170	570	170	<b>571</b>	<b>170</b>	8	545	178	547	177	<b>545</b>	<b>178</b>
462.libquantum	8	655	253	<b>652</b>	<b>254</b>	652	254	1	<b>71.7</b>	<b>289</b>	71.7	289	71.7	289
464.h264ref	8	<b>627</b>	<b>283</b>	626	283	627	282	8	595	297	597	296	<b>597</b>	<b>297</b>
471.omnetpp	8	693	72.1	<b>693</b>	<b>72.1</b>	693	72.1	8	<b>673</b>	<b>74.3</b>	673	74.3	673	74.3
473.astar	8	<b>622</b>	<b>90.3</b>	621	90.4	627	89.6	8	558	101	559	100	<b>559</b>	<b>100</b>
483.xalancbmk	8	<b>389</b>	<b>142</b>	389	142	389	142	8	<b>389</b>	<b>142</b>	389	142	389	142

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Submit Notes

The config file option 'submit' was used.  
taskset was used to bind processes to cores except  
for 462.libquantum peak

## Operating System Notes

'ulimit -s unlimited' was used to set the stacksize to unlimited prior to run  
OMP\_NUM\_THREADS set to number of processors  
KMP\_AFFINITY set to "physical,0"  
KMP\_STACKSIZE set to 64M

## Platform Notes

BIOS configuration:  
Adjacent Cache Line Prefetch Disabled

## Base Compiler Invocation

C benchmarks:  
icc

C++ benchmarks:  
icpc



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## Base Portability Flags

400.perlbench: -DSPEC\_CPU\_LINUX\_IA32  
462.libquantum: -DSPEC\_CPU\_LINUX  
483.xalancbmk: -DSPEC\_CPU\_LINUX

## Base Optimization Flags

C benchmarks:

-xSSE4.1 -ipo -O3 -no-prec-div -static -inline-calloc  
-opt-malloc-options=3 -opt-prefetch

C++ benchmarks:

-xSSE4.1 -ipo -O3 -no-prec-div -opt-prefetch -Wl,-z,muldefs  
-L/spec/cpu2006.1.1/lib -lsmartheap

## Base Other Flags

C benchmarks:

403.gcc: -Dalloca=\_alloca

## Peak Compiler Invocation

C benchmarks (except as noted below):

icc

401.bzip2: /opt/intel/Compiler/11.0/042/bin/intel64/icc  
-L/opt/intel/Compiler/11.0/042/ipp/em64t/lib  
-I/opt/intel/Compiler/11.0/042/ipp/em64t/include

456.hmmer: /opt/intel/Compiler/11.0/042/bin/intel64/icc  
-L/opt/intel/Compiler/11.0/042/ipp/em64t/lib  
-I/opt/intel/Compiler/11.0/042/ipp/em64t/include

C++ benchmarks:

icpc

## Peak Portability Flags

400.perlbench: -DSPEC\_CPU\_LINUX\_IA32  
401.bzip2: -DSPEC\_CPU\_LP64  
456.hmmer: -DSPEC\_CPU\_LP64

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## Peak Portability Flags (Continued)

462.libquantum: -DSPEC\_CPU\_LINUX  
483.xalancbmk: -DSPEC\_CPU\_LINUX

## Peak Optimization Flags

C benchmarks:

400.perlbench: -prof-gen(pass 1) -prof-use(pass 2) -xSSE4.1 -ipo -O3  
-no-prec-div -static -ansi-alias -opt-prefetch

401.bzip2: -prof-gen(pass 1) -prof-use(pass 2) -xSSE4.1 -ipo -O3  
-no-prec-div -static -opt-prefetch -ansi-alias

403.gcc: -xSSE4.1 -ipo -O3 -no-prec-div -static -inline-calloc  
-opt-malloc-options=3

429.mcf: basepeak = yes

445.gobmk: -prof-gen(pass 1) -prof-use(pass 2) -xSSE4.1 -O2 -ipo  
-no-prec-div -ansi-alias

456.hmmer: -xSSE4.1 -ipo -O3 -no-prec-div -static -unroll2  
-ansi-alias

458.sjeng: -prof-gen(pass 1) -prof-use(pass 2) -xSSE4.1 -ipo -O3  
-no-prec-div -static -unroll4

462.libquantum: -xSSE4.1 -ipo -O3 -no-prec-div -static  
-opt-malloc-options=3 -parallel -par-runtime-control  
-opt-prefetch

464.h264ref: -prof-gen(pass 1) -prof-use(pass 2) -xSSE4.1 -ipo -O3  
-no-prec-div -static -unroll2 -ansi-alias

C++ benchmarks:

471.omnetpp: -prof-gen(pass 1) -prof-use(pass 2) -xSSE4.1 -ipo -O3  
-no-prec-div -ansi-alias -opt-ra-region-strategy=block  
-Wl,-z,muldefs -L/spec/cpu2006.1.1/lib -lsmarheap

473.astar: -prof-gen(pass 1) -prof-use(pass 2) -xSSE4.1 -ipo -O3  
-no-prec-div -ansi-alias -opt-ra-region-strategy=routine  
-Wl,-z,muldefs -L/spec/cpu2006.1.1/lib -lsmarheap

483.xalancbmk: basepeak = yes



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## Peak Other Flags

C benchmarks:

403.gcc: -Dalloca=\_alloca

The flags file that was used to format this result can be browsed at

<http://www.spec.org/cpu2006/flags/Intel-ic11.0-int-linux64-revD.html>

You can also download the XML flags source by saving the following link:

<http://www.spec.org/cpu2006/flags/Intel-ic11.0-int-linux64-revD.xml>

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For other inquiries, please contact [webmaster@spec.org](mailto:webmaster@spec.org).

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