



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2024 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C220 M7 (Intel Xeon Silver 4516Y+, 2.20GHz)

SPECspeed®2017_int_base = 13.4

SPECspeed®2017_int_peak = 13.7

CPU2017 License: 9019

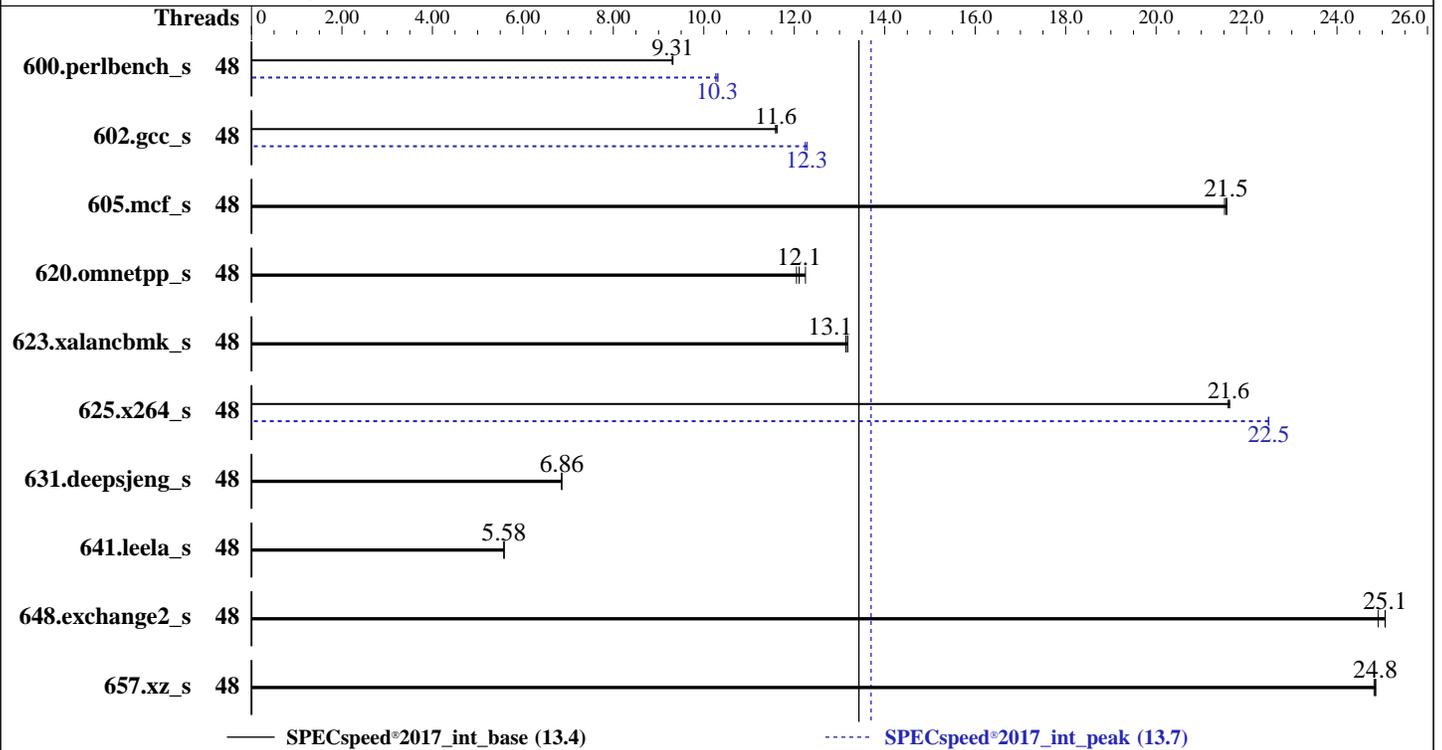
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jul-2024

Hardware Availability: Feb-2024

Software Availability: Dec-2023



Hardware

CPU Name: Intel Xeon Silver 4516Y+
 Max MHz: 3700
 Nominal: 2200
 Enabled: 48 cores, 2 chips
 Orderable: 1,2 Chips
 Cache L1: 32 KB I + 48 KB D on chip per core
 L2: 2 MB I+D on chip per core
 L3: 45 MB I+D on chip per chip
 Other: None
 Memory: 1 TB (16 x 64 GB 2Rx4 PC5-5600B-R, running at 4400)
 Storage: 1 x 960 GB M.2 SSD SATA
 Other: CPU Cooling: Air

Software

OS: SUSE Linux Enterprise Server 15 SP4
 5.14.21-150400.22-default
 Compiler: C/C++: Version 2024.1 of Intel oneAPI DPC++/C++ Compiler for Linux;
 Fortran: Version 2024.1 of Intel Fortran Compiler for Linux;
 Parallel: Yes
 Firmware: Version 4.3.3a released Jan-2024
 File System: btrfs
 System State: Run level 3 (multi-user)
 Base Pointers: 64-bit
 Peak Pointers: 64-bit
 Other: jemalloc memory allocator V5.0.1
 Power Management: BIOS set to prefer power save with minimal impact on performance



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2024 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C220 M7 (Intel Xeon Silver 4516Y+, 2.20GHz)

SPECspeed®2017_int_base = 13.4

SPECspeed®2017_int_peak = 13.7

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jul-2024
Hardware Availability: Feb-2024
Software Availability: Dec-2023

Results Table

Benchmark	Base							Peak						
	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
600.perlbench_s	48	190	9.32	191	9.30	<u>191</u>	<u>9.31</u>	48	<u>172</u>	<u>10.3</u>	172	10.3	173	10.3
602.gcc_s	48	344	11.6	343	11.6	344	11.6	48	324	12.3	324	12.3	325	12.2
605.mcf_s	48	219	21.6	219	21.5	<u>219</u>	<u>21.5</u>	48	219	21.6	219	21.5	<u>219</u>	<u>21.5</u>
620.omnetpp_s	48	135	12.1	133	12.2	135	12.0	48	135	12.1	133	12.2	135	12.0
623.xalancbmk_s	48	108	13.1	108	13.1	107	13.2	48	108	13.1	108	13.1	107	13.2
625.x264_s	48	81.7	21.6	81.6	21.6	<u>81.7</u>	<u>21.6</u>	48	78.4	22.5	78.4	22.5	78.5	22.5
631.deepsjeng_s	48	<u>209</u>	6.86	209	6.85	209	6.86	48	<u>209</u>	6.86	209	6.85	209	6.86
641.leela_s	48	306	5.58	306	5.58	306	5.58	48	306	5.58	306	5.58	306	5.58
648.exchange2_s	48	<u>117</u>	25.1	117	25.1	118	24.9	48	<u>117</u>	25.1	117	25.1	118	24.9
657.xz_s	48	<u>249</u>	24.8	249	24.8	249	24.9	48	<u>249</u>	24.8	249	24.8	249	24.9

SPECspeed®2017_int_base = 13.4

SPECspeed®2017_int_peak = 13.7

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOCONF = "retain:true"
OMP_STACKSIZE = "192M"

General Notes

Binaries compiled on a system with 2x Intel Xeon Platinum 8280M CPU + 384GB RAM
memory using Redhat Enterprise Linux 8.0
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5
sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2024 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C220 M7 (Intel Xeon Silver 4516Y+, 2.20GHz)

SPECspeed®2017_int_base = 13.4

SPECspeed®2017_int_peak = 13.7

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jul-2024

Hardware Availability: Feb-2024

Software Availability: Dec-2023

Platform Notes

BIOS Settings:

Intel Hyper-Threading Technology set to Disabled
Sub NUMA Clustering set to Disabled
LLC Dead Line set to Disabled
ADDDC Sparing set to Disabled
Processor C6 Report set to Enabled
UPI Power Management set to Enabled
Enhanced CPU performance set to Auto

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6732 of 2022-11-07 fe91c89b7ed5c36ae2c92cc097bec197
running on localhost Tue Jul 23 23:23:17 2024

SUT (System Under Test) info as seen by some common utilities.

----- Table of contents -----

1. uname -a
2. w
3. Username
4. ulimit -a
5. sysinfo process ancestry
6. /proc/cpuinfo
7. lscpu
8. numactl --hardware
9. /proc/meminfo
10. who -r
11. Systemd service manager version: systemd 249 (249.11+suse.124.g2bc0b2c447)
12. Services, from systemctl list-unit-files
13. Linux kernel boot-time arguments, from /proc/cmdline
14. cpupower frequency-info
15. sysctl
16. /sys/kernel/mm/transparent_hugepage
17. /sys/kernel/mm/transparent_hugepage/khugepaged
18. OS release
19. Disk information
20. /sys/devices/virtual/dmi/id
21. dmidecode
22. BIOS

1. uname -a
Linux localhost 5.14.21-150400.22-default #1 SMP PREEMPT_DYNAMIC Wed May 11 06:57:18 UTC 2022 (49db222)
x86_64 x86_64 x86_64 GNU/Linux

2. w
23:23:17 up 20 min, 1 user, load average: 0.08, 0.03, 0.05
USER TTY FROM LOGIN@ IDLE JCPU PCPU WHAT
root tty1 - 23:23 5.00s 1.21s 0.16s -bash

3. Username
From environment variable \$USER: root

4. ulimit -a

(Continued on next page)



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2024 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C220 M7 (Intel Xeon Silver 4516Y+, 2.20GHz)

SPECspeed®2017_int_base = 13.4

SPECspeed®2017_int_peak = 13.7

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jul-2024
Hardware Availability: Feb-2024
Software Availability: Dec-2023

Platform Notes (Continued)

```

core file size      (blocks, -c) unlimited
data seg size      (kbytes, -d) unlimited
scheduling priority (-e) 0
file size          (blocks, -f) unlimited
pending signals    (-i) 4126994
max locked memory  (kbytes, -l) 64
max memory size    (kbytes, -m) unlimited
open files         (-n) 1024
pipe size          (512 bytes, -p) 8
POSIX message queues (bytes, -q) 819200
real-time priority (-r) 0
stack size         (kbytes, -s) unlimited
cpu time           (seconds, -t) unlimited
max user processes (-u) 4126994
virtual memory     (kbytes, -v) unlimited
file locks         (-x) unlimited

```

```

-----
5. sysinfo process ancestry
/usr/lib/systemd/systemd --switched-root --system --deserialize 30
login -- root
-bash
-bash
runcpu --define default-platform-flags -c ic2024.1-lin-sapphirerapids-speed-20240308.cfg --define cores=48
--tune all -o all --define drop_caches intspeed
runcpu --define default-platform-flags --configfile ic2024.1-lin-sapphirerapids-speed-20240308.cfg --define
cores=48 --tune all --output_format all --define drop_caches --nopower --runmode speed --tune base:peak
--size refspeed intspeed --nopreenv --note-preenv --logfile
$SPEC/tmp/CPU2017.125/templogs/preenv.intspeed.125.0.log --lognum 125.0 --from_runcpu 2
specperl $SPEC/bin/sysinfo
$SPEC = /home/cpu2017

```

```

-----
6. /proc/cpuinfo
model name      : INTEL(R) XEON(R) SILVER 4516Y+
vendor_id      : GenuineIntel
cpu family     : 6
model          : 207
stepping       : 2
microcode      : 0x21000200
bugs           : spectre_v1 spectre_v2 spec_store_bypass swappg
cpu cores      : 24
siblings       : 24
2 physical ids (chips)
48 processors (hardware threads)
physical id 0: core ids 0-23
physical id 1: core ids 0-23
physical id 0: apicids 0,2,4,6,8,10,12,14,16,18,20,22,24,26,28,30,32,34,36,38,40,42,44,46
physical id 1: apicids
128,130,132,134,136,138,140,142,144,146,148,150,152,154,156,158,160,162,164,166,168,170,172,174
Caution: /proc/cpuinfo data regarding chips, cores, and threads is not necessarily reliable, especially for
virtualized systems. Use the above data carefully.

```

```

-----
7. lscpu

From lscpu from util-linux 2.37.2:
Architecture:      x86_64
CPU op-mode(s):    32-bit, 64-bit
Address sizes:      46 bits physical, 57 bits virtual

```

(Continued on next page)



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2024 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C220 M7 (Intel Xeon Silver 4516Y+, 2.20GHz)

SPECspeed®2017_int_base = 13.4

SPECspeed®2017_int_peak = 13.7

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jul-2024
Hardware Availability: Feb-2024
Software Availability: Dec-2023

Platform Notes (Continued)

```

Byte Order:                Little Endian
CPU(s):                    48
On-line CPU(s) list:      0-47
Vendor ID:                 GenuineIntel
Model name:               INTEL(R) XEON(R) SILVER 4516Y+
CPU family:               6
Model:                    207
Thread(s) per core:       1
Core(s) per socket:       24
Socket(s):                2
Stepping:                 2
CPU max MHz:              3700.0000
CPU min MHz:              800.0000
BogoMIPS:                 4400.00
Flags:                    fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36
                          clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
                          lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology
                          nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor
                          ds_cpl smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2
                          x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm
                          abm 3dnowprefetch cpuid_fault epb cat_l3 cat_l2 cdp_l3 invpcid_single
                          cdp_l2 ssbd mba ibrs ibpb stibp ibrs_enhanced fsgsbase tsc_adjust bmi1 hle
                          avx2 smep bmi2 erms invpcid rtm cqm rdt_a avx512f avx512dq rdseed adx smap
                          avx512ifma clflushopt clwb intel_pt avx512cd sha_ni avx512bw avx512vl
                          xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total
                          cqm_mbm_local avx_vnni avx512_bf16 wbnoinvd dtherm ida arat pln pts hwp
                          hwp_act_window hwp_epp hwp_pkg_req avx512vbmi umip pku ospke waitpkg
                          avx512_vbmi2 gfni vaes vpclmulqdq avx512_vnni avx512_bitalg tme
                          avx512_vpopcntdq la57 rdpid bus_lock_detect cldemote movdiri movdir64b
                          enqcmd fsrm md_clear serialize tsxldtrk pconfig arch_lbr avx512_fp16
                          amx_tile flush_l1d arch_capabilities
L1d cache:                2.3 MiB (48 instances)
L1i cache:                1.5 MiB (48 instances)
L2 cache:                 96 MiB (48 instances)
L3 cache:                 90 MiB (2 instances)
NUMA node(s):             2
NUMA node0 CPU(s):       0-23
NUMA node1 CPU(s):       24-47
Vulnerability Itlb multihit: Not affected
Vulnerability L1tf:       Not affected
Vulnerability Mds:        Not affected
Vulnerability Meltdown:   Not affected
Vulnerability Spec store bypass: Mitigation; Speculative Store Bypass disabled via prctl and seccomp
Vulnerability Spectre v1:  Mitigation; usercopy/swapgs barriers and __user pointer sanitization
Vulnerability Spectre v2:  Mitigation; Enhanced IBRS, IBPB conditional, RSB filling
Vulnerability Srbds:      Not affected
Vulnerability Tsx async abort: Not affected

```

From lscpu --cache:

NAME	ONE-SIZE	ALL-SIZE	WAYS	TYPE	LEVEL	SETS	PHY-LINE	COHERENCY-SIZE
L1d	48K	2.3M	12	Data	1	64	1	64
L1i	32K	1.5M	8	Instruction	1	64	1	64
L2	2M	96M	16	Unified	2	2048	1	64
L3	45M	90M	15	Unified	3	49152	1	64

8. numactl --hardware

NOTE: a numactl 'node' might or might not correspond to a physical chip.

available: 2 nodes (0-1)

node 0 cpus: 0-23

(Continued on next page)



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2024 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C220 M7 (Intel Xeon Silver 4516Y+, 2.20GHz)

SPECspeed®2017_int_base = 13.4

SPECspeed®2017_int_peak = 13.7

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jul-2024
Hardware Availability: Feb-2024
Software Availability: Dec-2023

Platform Notes (Continued)

```
node 0 size: 515737 MB
node 0 free: 514164 MB
node 1 cpus: 24-47
node 1 size: 516035 MB
node 1 free: 515453 MB
node distances:
node 0 1
0: 10 21
1: 21 10
```

9. /proc/meminfo
MemTotal: 1056535096 kB

10. who -r
run-level 3 Jul 23 23:03

11. Systemd service manager version: systemd 249 (249.11+suse.124.g2bc0b2c447)
Default Target Status
multi-user running

12. Services, from systemctl list-unit-files

STATE	UNIT FILES
enabled	YaST2-Firstboot YaST2-Second-Stage apparmor auditd cron getty@ haveged irqbalance iscsi issue-generator kbdsettings klog libvirtd lvm2-monitor nscd postfix purge-kernels rollback rsyslog smartd sshd wicked wickedd-auto4 wickedd-dhcp4 wickedd-dhcp6 wickedd-nanny
enabled-runtime	systemd-remount-fs
disabled	autofs autoyast-initscripts blk-availability boot-sysctl ca-certificates chrony-wait chronyd console-getty cups cups-browsed debug-shell dnsmasq ebttables exchange-bmc-os-info firewalld gpm grub2-once haveged-switch-root ipmi ipmievdev iscsi-init iscsid issue-add-ssh-keys kdump kdump-early kexec-load ksm kvm_stat libvirt-guests lunmask man-db-create multipathd nfs nfs-blkmap nfs-server nfsserver rdisc rpcbind rpmconfigcheck rsyncd serial-getty@ smartd_generate_opts snmpd snmptrapd strongswan strongswan-starter svnserve systemd-boot-check-no-failures systemd-network-generator systemd-nspawn@ systemd-sysexec systemd-time-wait-sync systemd-timesyncd tcsd udisks2 virtinterfaced virtnetworkd virtnodevdev virtnwfilterd virtproxyd virtqemu virtsecret virtstorage d pcsd virtlockd virtlogd wickedd
indirect	

13. Linux kernel boot-time arguments, from /proc/cmdline
BOOT_IMAGE=/boot/vmlinuz-5.14.21-150400.22-default
root=UUID=2e0ad397-074a-46f8-9f0a-5231b03b9d87
splash=silent
mitigations=auto
quiet
security=apparmor

14. cpupower frequency-info
analyzing CPU 0:
current policy: frequency should be within 800 MHz and 3.70 GHz.
The governor "performance" may decide which speed to use within this range.
boost state support:
Supported: yes
Active: yes

(Continued on next page)



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2024 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C220 M7 (Intel Xeon Silver 4516Y+, 2.20GHz)

SPECspeed®2017_int_base = 13.4

SPECspeed®2017_int_peak = 13.7

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jul-2024

Hardware Availability: Feb-2024

Software Availability: Dec-2023

Platform Notes (Continued)

15. sysctl

```

kernel.numa_balancing          1
kernel.randomize_va_space     2
vm.compaction_proactiveness   20
vm.dirty_background_bytes     0
vm.dirty_background_ratio     10
vm.dirty_bytes                 0
vm.dirty_expire_centisecs    3000
vm.dirty_ratio                 20
vm.dirty_writeback_centisecs  500
vm.dirtytime_expire_seconds   43200
vm.extfrag_threshold          500
vm.min_unmapped_ratio         1
vm.nr_hugepages                0
vm.nr_hugepages_mempolicy     0
vm.nr_overcommit_hugepages    0
vm.swappiness                   1
vm.watermark_boost_factor     15000
vm.watermark_scale_factor     10
vm.zone_reclaim_mode          0

```

16. /sys/kernel/mm/transparent_hugepage

```

defrag          [always] defer defer+madvise madvise never
enabled        [always] madvise never
hpage_pmd_size 2097152
shmem_enabled  always within_size advise [never] deny force

```

17. /sys/kernel/mm/transparent_hugepage/khugepaged

```

alloc_sleep_millisecs  60000
defrag                  1
max_ptes_none          511
max_ptes_shared        256
max_ptes_swap          64
pages_to_scan          4096
scan_sleep_millisecs  10000

```

18. OS release

```

From /etc/*-release /etc/*-version
os-release SUSE Linux Enterprise Server 15 SP4

```

19. Disk information

```

SPEC is set to: /home/cpu2017
Filesystem      Type  Size  Used Avail Use% Mounted on
/dev/sda2       btrfs 445G  22G  423G   5% /home

```

20. /sys/devices/virtual/dmi/id

```

Vendor:      Cisco Systems Inc
Product:     UCSC-C220-M7S
Serial:      WZP2702091W

```

21. dmidecode

```

Additional information from dmidecode 3.2 follows.  WARNING: Use caution when you interpret this section.
The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately

```

(Continued on next page)



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2024 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C220 M7 (Intel Xeon Silver 4516Y+, 2.20GHz)

SPECspeed®2017_int_base = 13.4

SPECspeed®2017_int_peak = 13.7

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jul-2024

Hardware Availability: Feb-2024

Software Availability: Dec-2023

Platform Notes (Continued)

determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:

16x 0xCE00 M321R8GA0PB0-CWMCH 64 GB 2 rank 5600, configured at 4400

22. BIOS

(This section combines info from /sys/devices and dmidecode.)

BIOS Vendor: Cisco Systems, Inc.
BIOS Version: C220M7.4.3.3a.0.0118241337
BIOS Date: 01/18/2024
BIOS Revision: 5.32

Compiler Version Notes

C | 600.perlbench_s(base, peak) 602.gcc_s(base, peak) 605.mcf_s(base, peak) 625.x264_s(base, peak)
| 657.xz_s(base, peak)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2024.1.0 Build 20240308
Copyright (C) 1985-2024 Intel Corporation. All rights reserved.

C++ | 620.omnetpp_s(base, peak) 623.xalancbmk_s(base, peak) 631.deepsjeng_s(base, peak)
| 641.leela_s(base, peak)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2024.1.0 Build 20240308
Copyright (C) 1985-2024 Intel Corporation. All rights reserved.

Fortran | 648.exchange2_s(base, peak)

Intel(R) Fortran Compiler for applications running on Intel(R) 64, Version 2024.1.0 Build 20240308
Copyright (C) 1985-2024 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:

icx

C++ benchmarks:

icpx

Fortran benchmarks:

ifx



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2024 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C220 M7 (Intel Xeon Silver 4516Y+, 2.20GHz)

SPECspeed®2017_int_base = 13.4

SPECspeed®2017_int_peak = 13.7

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jul-2024

Hardware Availability: Feb-2024

Software Availability: Dec-2023

Base Portability Flags

```
600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64
```

Base Optimization Flags

C benchmarks:

```
-w -std=c11 -m64 -Wl,-z,muldefs -xsapphirerapids -O3 -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -fiopenmp
-DSPEC_OPENMP -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
```

C++ benchmarks:

```
-w -std=c++14 -m64 -Wl,-z,muldefs -xsapphirerapids -O3 -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
```

Fortran benchmarks:

```
-w -m64 -Wl,-z,muldefs -xsapphirerapids -O3 -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
```

Peak Compiler Invocation

C benchmarks:

icx

C++ benchmarks:

icpx

Fortran benchmarks:

ifx



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2024 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C220 M7 (Intel Xeon Silver 4516Y+, 2.20GHz)

SPECspeed®2017_int_base = 13.4

SPECspeed®2017_int_peak = 13.7

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jul-2024

Hardware Availability: Feb-2024

Software Availability: Dec-2023

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:

```
600.perlbench_s: -w -m64 -std=c11 -Wl,-z,muldefs
-fprofile-generate(pass 1)
-fprofile-use=default.profdata(pass 2) -xCORE-AVX2(pass 1)
-flto -Ofast(pass 1) -xCORE-AVX512 -O3 -ffast-math
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-fiopenmp -DSPEC_OPENMP -fno-strict-overflow
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

602.gcc_s: -w -m64 -std=c11 -Wl,-z,muldefs
-fprofile-generate(pass 1)
-fprofile-use=default.profdata(pass 2) -xCORE-AVX2(pass 1)
-flto -Ofast(pass 1) -xCORE-AVX512 -O3 -ffast-math
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-fiopenmp -DSPEC_OPENMP -L/usr/local/jemalloc64-5.0.1/lib
-ljemalloc

605.mcf_s: basepeak = yes

625.x264_s: -w -std=c11 -m64 -Wl,-z,muldefs -xsapphirerapids -O3
-ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -fiopenmp -DSPEC_OPENMP
-fno-alias -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

657.xz_s: basepeak = yes
```

C++ benchmarks:

```
620.omnetpp_s: basepeak = yes

623.xalancbmk_s: basepeak = yes

631.deepsjeng_s: basepeak = yes

641.leela_s: basepeak = yes
```

Fortran benchmarks:

(Continued on next page)



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2024 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C220 M7 (Intel Xeon Silver 4516Y+, 2.20GHz)

SPECspeed®2017_int_base = 13.4

SPECspeed®2017_int_peak = 13.7

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jul-2024

Hardware Availability: Feb-2024

Software Availability: Dec-2023

Peak Optimization Flags (Continued)

648.exchange2_s:basepeak = yes

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic2024-official-linux64.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.0-EMR-revD.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic2024-official-linux64.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.0-EMR-revD.xml>

SPEC CPU and SPECspeed are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.9 on 2024-07-23 23:23:16-0400.

Report generated on 2024-08-14 14:03:04 by CPU2017 PDF formatter v6716.

Originally published on 2024-08-13.