Cisco Systems

Cisco UCS C225 M6 (AMD EPYC 7773X 64-Core)

| SPECrate®2017_int_base = 427 |
| SPECrate®2017_int_peak = 460 |

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Feb-2022
Hardware Availability: Mar-2022
Software Availability: Dec-2021

### Hardware

- **CPU Name:** AMD EPYC 7773X
- **Max MHz:** 3500
- **Nominal:** 2200
- **Enabled:** 64 cores, 1 chip, 2 threads/core
- **Orderable:** 1 chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
  - **L1:** 512 KB I+D on chip per core
  - **L3:** 768 MB I+D on chip per chip, 96 MB shared / 8 cores
- **Other:** None
- **Memory:** 1 TB (8 x 128 GB 4Rx4 PC4-3200V-L)
- **Storage:** 1 x 1.6 TB SSD SATA
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 15 SP3 (x86_64) kernel version 5.3.18-57-default
- **Compiler:** C/C++/Fortran: Version 3.2.0 of AOCC
- **Parallel:** No
- **Firmware:** Version 4.2.1.26 released Jan-2022
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 32/64-bit
- **Other:** jemalloc: jemalloc memory allocator library v5.1.0
- **Power Management:** BIOS and OS set to prefer performance at the cost of additional power usage
Cisco Systems
Cisco UCS C225 M6 (AMD EPYC 7773X 64-Core)

SPEC CPU®2017 Integer Rate Result

Copyright 2017-2022 Standard Performance Evaluation Corporation

**Results Table**

<table>
<thead>
<tr>
<th>Benchmark</th>
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<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
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<tbody>
<tr>
<td>500.perlbench_r</td>
<td>128</td>
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<td>520.omnetpp_r</td>
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<td>523.xalancbmk_r</td>
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<td>438</td>
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<td>435</td>
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</table>

**Compiler Notes**

The AMD64 AOCC Compiler Suite is available at http://developer.amd.com/amd-aocc/

**Submit Notes**

The config file option 'submit' was used.

'numactl' was used to bind copies to the cores.

See the configuration file for details.

**Operating System Notes**

'ulimit -s unlimited' was used to set environment stack size limit

'ulimit -l 2097152' was used to set environment locked pages in memory limit

runcpu command invoked through numactl i.e.:

```
numactl --interleave=all runcpu <etc>
```

To limit dirty cache to 8% of memory, 'syscall -w vm.dirty_ratio=8' run as root.

To limit swap usage to minimum necessary, 'syscall -w vm.swappiness=1' run as root.

To free node-local memory and avoid remote memory usage,

'sysctl -w vm.zone_reclaim_mode=1' run as root.

To clear filesystem caches, 'sync; sysctl -w vm.drop_caches=3' run as root.

To disable address space layout randomization (ASLR) to reduce run-to-run variability, 'syscall -w kernel.randomize_va_space=0' run as root.

(Continued on next page)
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Cisco UCS C225 M6 (AMD EPYC 7773X 64-Core)  

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Operating System Notes (Continued)

To enable Transparent Hugepages (THP) only on request for base runs,  
'echo madvise > /sys/kernel/mm/transparent_hugepage/enabled' run as root.  
To enable THP for all allocations for peak runs,  
'echo always > /sys/kernel/mm/transparent_hugepage/enabled' and  
'echo always > /sys/kernel/mm/transparent_hugepage/defrag' run as root.

Environment Variables Notes

Environment variables set by runcpu before the start of the run:  
LD_LIBRARY_PATH =  
"/home/cpu2017/amd_rate_aocc320_milanx_A_lib/lib;/home/cpu2017/amd_rate_aocc320_milanx_A_lib/lib32:"  
MALLOC_CONF = "retain:true"

Environment variables set by runcpu during the 523.xalancbmk_r peak run:  
MALLOC_CONF = "thp:never"

General Notes

Binaries were compiled on a system with 2x AMD EPYC 7742 CPU + 1TiB Memory using OpenSUSE 15.2

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)  
is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)  
is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)  
is mitigated in the system as tested and documented.

jemalloc: configured and built with GCC v4.8.2 in RHEL 7.4 (No options specified)  
jemalloc 5.1.0 is available here:  
https://github.com/jemalloc/jemalloc/releases/download/5.1.0/jemalloc-5.1.0.tar.bz2

Platform Notes

BIOS Configuration  
SMT Mode set to Auto  
NUMA nodes per socket set to NPS4  
ACPI SRAT L3 Cache As NUMA Domain set to Enabled  
DRAM Scrub Time set to Disabled  
Determinism Slider set to Power  
Memory Interleaving set to Disabled

(Continued on next page)
Platform Notes (Continued)

APBDIS set to 1

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16aca6d4
running on localhost Tue Apr 19 17:13:35 2022

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : AMD EPYC 7773X 64-Core Processor
1 "physical id"s (chips)
128 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 64
siblings : 128
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52
53 54 55 56 57 58 59 60 61 62 63

From lscpu from util-linux 2.36.2:
Architecture:                    x86_64
CPU op-mode(s):                  32-bit, 64-bit
Byte Order:                      Little Endian
Address sizes:                   48 bits physical, 48 bits virtual
CPU(s):                          128
On-line CPU(s) list:             0-127
Thread(s) per core:              2
Core(s) per socket:              64
Socket(s):                       1
NUMA node(s):                    8
Vendor ID:                       AuthenticAMD
CPU family:                      25
Model:                           1
Model name:                      AMD EPYC 7773X 64-Core Processor
Stepping:                        2
Frequency boost:                 enabled
CPU MHz:                         1796.245
CPU max MHz:                     2200.0000
CPU min MHz:                     1500.0000
BogoMIPS:                        4391.79
Virtualization:                  AMD-V
L1d cache:                       2 MiB
L1i cache:                       2 MiB
L2 cache:                        32 MiB

(Continued on next page)
Cisco Systems

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Platform Notes (Continued)

L3 cache: 768 MiB
NUMA node0 CPU(s): 0-7,64-71
NUMA node1 CPU(s): 8-15,72-79
NUMA node2 CPU(s): 16-23,80-87
NUMA node3 CPU(s): 24-31,88-95
NUMA node4 CPU(s): 32-39,96-103
NUMA node5 CPU(s): 40-47,104-111
NUMA node6 CPU(s): 48-55,112-119
NUMA node7 CPU(s): 56-63,120-127

Vulnerability Itlb multihit: Not affected
Vulnerability L1tf: Not affected
Vulnerability Mds: Not affected
Vulnerability Meltdown: Not affected
Vulnerability Spec store bypass: Mitigation; Speculative Store Bypass disabled via prctl and seccomp
Vulnerability Spectre v1: Mitigation; usercopy/swapgs barriers and __user pointer sanitation
Vulnerability Spectre v2: Mitigation; Full AMD retpoline, IBPB conditional, IBRS_FW, STIBP always-on, RSB filling
Vulnerability Srbds: Not affected
Vulnerability Tsx async abort: Not affected

Flags:

From lscpu --cache:
NAME ONE-SIZE ALL-SIZE WAYS TYPE LEVEL SETS PHY-LINE COHERENCY-SIZE
L1d 32K 2M 8 Data 1 64 1 64
L1i 32K 2M 8 Instruction 1 64 1 64
L2 512K 32M 8 Unified 2 1024 1 64
L3 96M 768M 16 Unified 3 98304 1 64

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
Cisco Systems

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</table>

Platform Notes (Continued)

<table>
<thead>
<tr>
<th>node</th>
<th>cpus:</th>
<th>size:</th>
<th>free:</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0 1 2 3 4 5 6 7 64 65 66 67 68 69 70 71</td>
<td>128836 MB</td>
<td>128277 MB</td>
</tr>
<tr>
<td>1</td>
<td>8 9 10 11 12 13 14 15 72 73 74 75 76 77 78 79</td>
<td>129018 MB</td>
<td>128514 MB</td>
</tr>
<tr>
<td>2</td>
<td>16 17 18 19 20 21 22 23 80 81 82 83 84 85 86 87</td>
<td>129020 MB</td>
<td>128289 MB</td>
</tr>
<tr>
<td>3</td>
<td>24 25 26 27 28 29 30 31 88 89 90 91 92 93 94 95</td>
<td>128984 MB</td>
<td>128514 MB</td>
</tr>
<tr>
<td>4</td>
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<td>128529 MB</td>
</tr>
<tr>
<td>5</td>
<td>40 41 42 43 44 45 46 47 104 105 106 107 108 109 110 111</td>
<td>129018 MB</td>
<td>128545 MB</td>
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<tr>
<td>6</td>
<td>48 49 50 51 52 53 54 55 112 113 114 115 116 117 118 119</td>
<td>129020 MB</td>
<td>128506 MB</td>
</tr>
<tr>
<td>7</td>
<td>56 57 58 59 60 61 62 63 120 121 122 123 124 125 126 127</td>
<td>129005 MB</td>
<td>128487 MB</td>
</tr>
</tbody>
</table>

From /proc/meminfo

MemTotal: 1056688388 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*

os-release:
NAME="SLES"

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Platform Notes (Continued)

VERSION="15-SP3"
VERSION_ID="15.3"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP3"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp3"

uname -a:
Linux localhost 5.3.18-57-default #1 SMP Wed Apr 28 10:54:41 UTC 2021 (ba3c2e9) x86_64
x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Mitigation: Speculative Store
CVE-2018-3639 (Speculative Store Bypass): Bypass disabled via prctl and
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapsgs
CVE-2017-5715 (Spectre variant 2): barriers and __user pointer
CVE-2020-0543 (Special Register Buffer Data Sampling): Mitigation: Full AMD retpoline,
CVE-2019-11135 (TSX Asynchronous Abort): IBPB: conditional, IBRS_FW, STIBP:
run-level 3 Apr 17 22:35
always-on, RSB filling

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/nvme0n1p3 xfs 1.5T 13G 1.5T 1% /

From /sys/devices/virtual/dmi/id
Vendor: Cisco Systems Inc
Product: UCSC-C225-M6N
Serial: WZP25230TMY

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you
interpret this section. The 'dmidecode' program reads system data which is "intended to
allow hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
8x 0xCE00 M386AAG40AM3-CWE 128 GB 4 rank 3200

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### Platform Notes (Continued)

**BIOS:**
- **BIOS Vendor:** Cisco Systems, Inc.
- **BIOS Version:** C225M6.4.2.1.26.0116222143
- **BIOS Date:** 01/16/2022
- **BIOS Revision:** 5.22

*(End of data from sysinfo program)*

### Compiler Version Notes

```
C       | 502.gcc_r(peak)
```

AMD clang version 13.0.0 (CLANG: A0CC_3.2.0-Build#128 2021_11_12) (based on LLVM Mirror.Version.13.0.0)  
Target: i386-unknown-linux-gnu  
Thread model: posix  
InstalledDir: /opt/AMD/aocc-compiler-3.2.0/bin

```
C       | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)
        | 525.x264_r(base, peak) 557.xz_r(base, peak)
```

AMD clang version 13.0.0 (CLANG: A0CC_3.2.0-Build#128 2021_11_12) (based on LLVM Mirror.Version.13.0.0)  
Target: x86_64-unknown-linux-gnu  
Thread model: posix  
InstalledDir: /opt/AMD/aocc-compiler-3.2.0/bin

```
C       | 502.gcc_r(peak)
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AMD clang version 13.0.0 (CLANG: A0CC_3.2.0-Build#128 2021_11_12) (based on LLVM Mirror.Version.13.0.0)  
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Target: x86_64-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.2.0/bin

C++ | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base)
    | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)

AMD clang version 13.0.0 (CLANG: AOCC_3.2.0-Build#128 2021_11_12) (based on LLVM Mirror.Version.13.0.0)
Target: i386-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.2.0/bin

C++ | 523.xalancbmk_r(peak)

AMD clang version 13.0.0 (CLANG: AOCC_3.2.0-Build#128 2021_11_12) (based on LLVM Mirror.Version.13.0.0)
Target: x86_64-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.2.0/bin

C++ | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base)
    | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)

AMD clang version 13.0.0 (CLANG: AOCC_3.2.0-Build#128 2021_11_12) (based on LLVM Mirror.Version.13.0.0)
Target: i386-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.2.0/bin

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Compiler Version Notes (Continued)

```
Fortran | 548.exchange2_r(base, peak)
```

AMD clang version 13.0.0 (CLANG: AOCC_3.2.0-Build#128 2021_11_12) (based on LLVM Mirror.Version.13.0.0)
Target: x86_64-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.2.0/bin

Base Compiler Invocation

C benchmarks:
clang
C++ benchmarks:
clang++
Fortran benchmarks:
flang

Base Portability Flags

- 500.perlbench_r: -DSPEC_LINUX_X64 -DSPEC_LP64
- 502.gcc_r: -DSPEC_LP64
- 505.mcf_r: -DSPEC_LP64
- 520.omnetpp_r: -DSPEC_LP64
- 523.xalancbmk_r: -DSPEC_LINUX -DSPEC_LP64
- 525.x264_r: -DSPEC_LP64
- 531.deepsjeng_r: -DSPEC_LP64
- 541.leela_r: -DSPEC_LP64
- 548.exchange2_r: -DSPEC_LP64
- 557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-m64 -Wl,-allow-multiple-definition -Wl,-mllvm -Wl,-enable-licm-vrp
-ffto -Wl,-mllvm -Wl,-region-vectorize

(Continued on next page)
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Cisco UCS C225 M6 (AMD EPYC 7773X 64-Core)

SPECrate®2017_int_base = 427
SPECrate®2017_int_peak = 460

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Feb-2022
Hardware Availability: Mar-2022
Software Availability: Dec-2021

Base Optimization Flags (Continued)

C benchmarks (continued):
- Wl,-mllvm -Wl,-function-specialize
- Wl,-mllvm -Wl,-align-all-nofallthru-blocks=6
- Wl,-mllvm -Wl,-reduce-array-computations=3
- Wl,-mllvm -Wl,-enable-loop-fusion -O3 -march=znver3 -fveclib=AMDLIBM
- ffast-math -fstruct-layout=5 -mllvm -unroll-threshold=50
- mllvm -inline-threshold=1000 -fremap-arrays
- mllvm -function-specialize -flv-function-specialization
- mllvm -enable-gvn-hoist -mllvm -global-vectorize-slp=true
- mllvm -enable-licm-vrp -mllvm -reduce-array-computations=3
- mllvm -enable-loop-fusion -z muldefs -lamdlibm -ljemalloc -lflang

C++ benchmarks:
- m64 -std=c++98 -flto -Wl,-mllvm -Wl,-region-vectorize
- Wl,-mllvm -Wl,-function-specialize
- Wl,-mllvm -Wl,-align-all-nofallthru-blocks=6
- Wl,-mllvm -Wl,-reduce-array-computations=3
- Wl,-mllvm -Wl,-enable-loop-fusion -O3 -march=znver3 -fveclib=AMDLIBM
- ffast-math -mllvm -enable-partial-unswitch
- mllvm -unroll-threshold=100 -finline-aggressive
- flv-function-specialization -mllvm -loop-unswitch-threshold=200000
- mllvm -reroll-loops -mllvm -aggressive-loop-unswitch
- mllvm -extra-vectorizer-passes -mllvm -reduce-array-computations=3
- mllvm -global-vectorize-slp=true -mllvm -convert-pow-exp-to-int=false
- mllvm -enable-loop-fusion -z muldefs -fvirtual-function-elimination
- fvisibility=hidden -lamdlibm -ljemalloc -lflang

Fortran benchmarks:
- m64 -Wl,-mllvm -Wl,-inline-recursion=4
- Wl,-mllvm -Wl,-isr-in-nested-loop -Wl,-mllvm -Wl,-enable-iv-split
- flto -Wl,-mllvm -Wl,-region-vectorize
- Wl,-mllvm -Wl,-function-specialize
- Wl,-mllvm -Wl,-align-all-nofallthru-blocks=6
- Wl,-mllvm -Wl,-reduce-array-computations=3
- Wl,-mllvm -Wl,-enable-loop-fusion -O3 -march=znver3 -fveclib=AMDLIBM
- ffast-math -z muldefs -mllvm -unroll-aggressive
- mllvm -unroll-threshold=500 -lamdlibm -ljemalloc -lflang

Base Other Flags

C benchmarks:
- Wno-unused-command-line-argument

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## Cisco Systems

Cisco UCS C225 M6 (AMD EPYC 7773X 64-Core)

### SPEC CPU®2017 Integer Rate Result

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>SPECrate®2017_int_peaks</th>
</tr>
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<tbody>
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**CPU2017 License:** 9019  
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**Test Date:** Feb-2022  
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### Base Other Flags (Continued)

- **C++ benchmarks:**  
  - -Wno-unused-command-line-argument

### Peak Compiler Invocation

- **C benchmarks:**  
  - clang

- **C++ benchmarks:**  
  - clang++

- **Fortran benchmarks:**  
  - flang

### Peak Portability Flags

- 500.perlbench_r: -DSPEC_LINUX_X64 -DSPEC_LP64
- 502.gcc_r: -D_FILE_OFFSET_BITS=64
- 505.mcf_r: -DSPEC_LP64
- 520.omnetpp_r: -DSPEC_LP64
- 523.xalancbmk_r: -DSPEC_LINUX -DSPEC_LP64
- 525.x264_r: -DSPEC_LP64
- 531.deepsjeng_r: -DSPEC_LP64
- 541.leea_r: -DSPEC_LP64
- 548.exchange2_r: -DSPEC_LP64
- 557.xz_r: -DSPEC_LP64

### Peak Optimization Flags

- **C benchmarks:**  
  - 500.perlbench_r: -m64 -Wl,-allow-multiple-definition  
    -Wl,-mllvm -Wl,-enable-licm-vrp -flto  
    -Wl,-mllvm -Wl,-function-specialize  
    -Wl,-mllvm -Wl,-align-all-nofallthru-blocks=6  
    -Wl,-mllvm -Wl,-reduce-array-computations=3  
    -fprofile-instr-generate(pass 1)  
    -fprofile-instr-use(pass 2) -Ofast -march=znver3  
    -fveclib=AMDLIBM -ffast-math -fstruct-layout=7  
    -mllvm -unroll-threshold=50 -fremap-arrays

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## Cisco Systems

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### SPEC CPU®2017 Integer Rate Result

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| Test Date:     | Feb-2022 |
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### Peak Optimization Flags (Continued)

500.perlbench_r (continued):

- `-mllvm -inline-threshold=1000`
- `-mllvm -enable-gvn-hoist`
- `-mllvm -global-vectorize-slp=false`
- `-mllvm -function-specialize`
- `-mllvm -enable-licm-vrp`
- `-mllvm -reduce-array-computations=3`
- `-lamdlibm -ljemalloc`

502.gcc_r: `-m32 -Wl,-allow-multiple-definition`

- `-Wl,-enable-licm-vrp -fhto`
- `-Wl,-mllvm -Wl,-function-specialize -Ofast -march=znver3`
- `-fveclib=AMDLIBM -ffast-math -fstruct-layout=7`
- `-mllvm -unroll-threshold=50 -fremap-arrays`
- `-mllvm -function-specialization -mllvm -inline-threshold=1000`
- `-mllvm -enable-gvn-hoist`
- `-mllvm -global-vectorize-slp=true`
- `-mllvm -function-specialize`
- `-mllvm -enable-licm-vrp`
- `-mllvm -reduce-array-computations=3`
- `-ljemalloc`

505.mcf_r: `-m64 -Wl,-allow-multiple-definition`

- `-Wl,-enable-licm-vrp -fhto`
- `-Wl,-mllvm -Wl,-function-specialize`
- `-Wl,-mllvm -Wl,-align-all-nofallthru-blocks=6`
- `-Wl,-mllvm -Wl,-reduce-array-computations=3 -Ofast`
- `-march=znver3 -fveclib=AMDLIBM -ffast-math -fstruct-layout=7`
- `-mllvm -unroll-threshold=50`
- `-fremap-arrays -mllvm -function-specialization`
- `-mllvm -inline-threshold=1000`
- `-mllvm -enable-gvn-hoist`
- `-mllvm -global-vectorize-slp=true`
- `-mllvm -function-specialize`
- `-mllvm -enable-licm-vrp`
- `-mllvm -reduce-array-computations=3`
- `-lamdlibm -ljemalloc`

525.x264_r: `basepeak = yes`

557.xz_r: `basepeak = yes`

C++ benchmarks:

520.omnetpp_r: `-m64 -std=c++98 -flto -Wl,-mllvm -Wl,-function-specialize`

- `-Wl,-mllvm -Wl,-align-all-nofallthru-blocks=6`
- `-Wl,-mllvm -Wl,-reduce-array-computations=3 -Ofast`
- `-march=znver3 -fveclib=AMDLIBM -ffast-math -finline-aggressive`
- `-fllvm-function-specialization`
- `-mllvm -unroll-threshold=100`
- `-mllvm -function-specialize`
- `-mllvm -enable-licm-vrp`
- `-mllvm -reduce-array-computations=3`
- `-mllvm -global-vectorize-slp=true`
- `-fvirtual-function-elimination -fvisibility=hidden`

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Cisco UCS C225 M6 (AMD EPYC 7773X 64-Core)

Peak Optimization Flags (Continued)

520.omnetpp_r (continued):
-landlibm -ljemalloc

523.xalancbmk_r: -m32 -Wl,-mllvm -Wl,-do-block-reorder=aggressive -flto
-Wl,-mllvm -Wl,-function-specialize
-Wl,-mllvm -Wl,-align-all-nofallthru-blocks=6
-Wl,-mllvm -Wl,-reduce-array-computations=3 -Ofast
-march=znver3 -fveclib=AMDLIBM -ffast-math
-finline-aggressive -mllvm -unroll-threshold=100
-flv-function-specialization -mllvm -enable-licm-vrp
-mllvm -reroil-loops -mllvm -aggressive-loop-unswitch
-mllvm -reduce-array-computations=3
-mllvm -global-vectorize-slp=true
-mllvm -do-block-reorder=aggressive
-fvirtual-function-elimination -fvisibility=hidden
-ljemalloc

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:
-m64 -Wl,-mllvm -Wl,-inline-recursion=4
-Wl,-mllvm -Wl,-lsr-in-nested-loop -Wl,-mllvm -Wl,-enable-iv-split
-flto -Wl,-mllvm -Wl,-function-specialize
-Wl,-mllvm -Wl,-align-all-nofallthru-blocks=6
-Wl,-mllvm -Wl,-reduce-array-computations=3 -O3 -march=znver3
-fveclib=AMDLIBM -ffast-math -mllvm -unroll-aggressive
-mllvm -unroll-threshold=500 -landlibm -ljemalloc -lflang

Peak Other Flags

C benchmarks (except as noted below):
- Wno-unused-command-line-argument

502.gcc_r: -L/usr/lib -Wno-unused-command-line-argument
-L/sppo/bin/cpu2017v118-aocc3-milanX/amd_rate_aocc320_milanx_A_lib/lib32

C++ benchmarks (except as noted below):
- Wno-unused-command-line-argument

523.xalancbmk_r: -L/usr/lib -Wno-unused-command-line-argument
-L/sppo/bin/cpu2017v118-aocc3-milanX/amd_rate_aocc320_milanx_A_lib/lib32
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The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/aocc320\textunderscore flags\textunderscore A1.html
http://www.spec.org/cpu2017/flags/Cisco\textunderscore Platform\textunderscore Settings\textunderscore AMD\textunderscore v2\textunderscore revD.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/aocc320\textunderscore flags\textunderscore A1.xml
http://www.spec.org/cpu2017/flags/Cisco\textunderscore Platform\textunderscore Settings\textunderscore AMD\textunderscore v2\textunderscore revD.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU\textsuperscript{\textregistered}2017 v1.1.8 on 2022-04-19 20:13:35-0400.
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