## Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Gold 6312U, 2.40GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base</th>
<th>186</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_fp_peak</td>
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**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Jan-2022  
**Hardware Availability:** Sep-2021  
**Software Availability:** Sep-2021

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</tbody>
</table>

### Hardware
- **CPU Name:** Intel Xeon Gold 6312U  
- **Max MHz:** 3600  
- **Nominal:** 2400  
- **Enabled:** 24 cores, 1 chip, 2 threads/core  
- **Orderable:** 1 Chip  
- **Cache L1:** 32 KB I + 48 KB D on chip per core  
- **L2:** 1.25 MB I+D on chip per core  
- **L3:** 36 MB I+D on chip per chip  
- **Memory:** 1 TB (16 x 64 GB 2Rx4 PC4-3200AA-R)  
- **Storage:** 1 x 240 GB M.2 SSD SATA  
- **Other:** None

### Software
- **OS:** SUSE Linux Enterprise Server 15 SP2 5.3.18-22-default  
- **Compiler:** C/C++: Version 2021.4.0 of Intel oneAPI DPC++/C++  
  Compiler Build 20210924 for Linux;  
  Fortran: Version 2021.4.0 of Intel Fortran  
  Compiler Classic Build 20210910 for Linux;  
- **Parallel:** No  
- **Firmware:** Version 5.0.1d released Aug-2021  
- **File System:** btrfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** Not Applicable  
- **Other:** jemalloc memory allocator V5.0.1  
- **Power Management:** OS set to prefer performance at the cost of additional power usage
### Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Gold 6312U, 2.40GHz)

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems

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</table>

**SPECrate®2017_fp_base = 186**  
**SPECrate®2017_fp_peak = Not Run**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes
Environment variables set by runcpu before the start of the run:

```
LD_LIBRARY_PATH = 
"/home/intel/tbb/2021.4.0/env/../lib/intel64/gcc4.8:/home/intel/mpi/2021 .4.0:/libfabric/lib:/home/intel/mpi/2021.4.0:/lib/release:/home/intel/mp i/2021.4.0:/lib:/home/intel/compiler/2021.4.0/linux/compiler/lib/intel64 _lin:/home/intel/compiler/2021.4.0/linux/lib:/home/intel/clck/2021.4.0/l lib/intel64:/home/cpu2017/je5.0.1-32"
MALLOCONF = "retain:true"
```
# SPEC CPU®2017 Floating Point Rate Result

## Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Gold 6312U, 2.40GHz)

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### General Notes

- Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM memory using openSUSE Leap 15.2
- Transparent Huge Pages enabled by default
- Prior to runcpu invocation
- Filesystem page cache synced and cleared with:
  ```bash
  sync; echo 3 > /proc/sys/vm/drop_caches
  ```
- numactl command invoked through numactl i.e.:
  ```bash
  numactl --interleave=all runcpu <etc>
  ```
- NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
- Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
- Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

### Platform Notes

- BIOS Settings:
  - Adjacent Cache Line Prefetcher set to Disabled
  - DCU Streamer Prefetch set to Disabled
  - Sub NUMA Clustering set to Enabled
  - LLC Dead Line set to Disabled
  - Memory Refresh Rate set to 1x Refresh
  - ADDDC Sparing set to Disabled
  - Patrol Scrub set to Disabled
  - Processor C6 Report set to Enabled

- Sysinfo program
  ```bash
  /home/cpu2017/bin/sysinfo
  ```
  Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d
  running on perf-blade6 Wed Jan 26 12:11:09 2022

- SUT (System Under Test) info as seen by some common utilities.
  For more information on this section, see
  ```bash
  https://www.spec.org/cpu2017/Docs/config.html#sysinfo
  ```

- From `/proc/cpuinfo`
  ```bash
  model name : Intel(R) Xeon(R) Gold 6312U CPU @ 2.40GHz
  1 "physical id"s (chips)
  48 "processors"
  cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from `/proc/cpuinfo might not be reliable. Use with caution.
  ```
  ```bash
  cpu cores : 24
  siblings : 48
  ```

(Continued on next page)
Cisco Systems

Cisco UCS X210c M6 (Intel Xeon Gold 6312U, 2.40GHz)

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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jan-2022
Hardware Availability: Sep-2021
Software Availability: Sep-2021

Platform Notes (Continued)

From lscpu from util-linux 2.33.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 48
On-line CPU(s) list: 0-47
Thread(s) per core: 2
Core(s) per socket: 24
Socket(s): 1
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Gold 6312U CPU @ 2.40GHz
Stepping: 6
CPU MHz: 3216.408
CPU max MHz: 3600.0000
CPU min MHz: 800.0000
BogoMIPS: 4800.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 36864K
NUMA node0 CPU(s): 0-11, 24-35
NUMA node1 CPU(s): 12-23, 36-47
Flags: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdaep1gb rtstsc lm constant-tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_ts cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes nxsave f16c rdrand lahf_lm abm 3nowprefetch cpuid_fault epb cat_13 invpcid_single ssbd mba ibrs ibpb ibrs_enhanced tpr_shadow vmni flexprility ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma ciflushopt clwb intel_pt avx512cd sha ni avx512bw avx512vl xsaveopt xsaves xsavec xgetbv1 xsavecs cqm_llc cqm_occnp lcc cqm_mbb_total cqm_mbb_local wbnoinvd dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req avx512vbm ulim pku ospke avx512_vmbi2 gfnv vaes vpcmldqd avx512_vnni avx512_bitalg tme avx512_vpopcntdq la57 rpdpid md_clear pconfig flush_l1d arch_capabilities

/proc/cpuinfo cache data
  cache size : 36864 KB

(Continued on next page)
Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Gold 6312U, 2.40GHz)

SPEC CPU®2017 Floating Point Rate Result

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECCrate®2017_fp_base = 186
SPECCrate®2017_fp_peak = Not Run

Test Date: Jan-2022
Hardware Availability: Sep-2021
Software Availability: Sep-2021

Platform Notes (Continued)

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 24 25 26 27 28 29 30 31 32 33 34 35
node 0 size: 515650 MB
node 0 free: 515126 MB
node 1 cpus: 12 13 14 15 16 17 18 19 20 21 22 23 36 37 38 39 40 41 42 43 44 45 46 47
node 1 size: 516086 MB
node 1 free: 515546 MB
node distances:
node 0 1
0: 10 11
1: 11 10

From /proc/meminfo
MemTotal: 1056498972 kB
HugePages_Total: 0
Hugepagesize: 2048 kB
/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release*/etc/*version*
os-release:
NAME="SLES"
VERSION="15-SP2"
VERSION_ID="15.2"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
Linux perf-blade6 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba)x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs

(Continued on next page)
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Platform Notes (Continued)

barriers and __user pointer sanitization
Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

CVE-2017-5715 (Spectre variant 2):

CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Jan 25 11:49

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda2 btrfs 222G 41G 181G 19% /home

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
  16x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200
  16x NO DIMM NO DIMM

BIOS:
  BIOS Vendor: Cisco Systems, Inc.
  BIOS Version: X210M6.5.0.1.0.0816211754
  BIOS Date: 08/16/2021
  BIOS Revision: 5.22

(End of data from sysinfo program)

Compiler Version Notes

C               | 519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)
------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
    Version 2021.4.0 Build 20210924
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.
------------------------------------------------------------------
C++           | 508.namd_r(base) 510.parest_r(base)

(Continued on next page)
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Compiler Version Notes (Continued)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.4.0 Build 20210924
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.

C++, C | 511.povray_r(base) 526.blender_r(base)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.4.0 Build 20210924
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.

C++, C, Fortran | 507.cactuBSSN_r(base)

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C++, C, Fortran | 507.cactuBSSN_r(base)

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C++, C, Fortran | 507.cactuBSSN_r(base)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.4.0 Build 20210924
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Fortran | 503.bwaves_r(base) 549.fotonik3d_r(base) 554.roms_r(base)

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.4.0 Build 20210910_000000
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Fortran, C | 521.wrf_r(base) 527.cam4_r(base)

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(Continued on next page)
Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Gold 6312U, 2.40GHz)

SPECrate®2017_fp_base = 186
SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Jan-2022
Hardware Availability: Sep-2021
Software Availability: Sep-2021

Compiler Version Notes (Continued)

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Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icx

Benchmarks using both C and C++:
icpx icx

Benchmarks using Fortran, C, and C++:
icpx icx ifort

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64
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Base Optimization Flags

C benchmarks:
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-fflto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc -L/home/cpu2017/je5.0.1-64

C++ benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc -L/home/cpu2017/je5.0.1-64

Fortran benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
-qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte
-mbranches-within-32B-boundaries -ljemalloc -L/home/cpu2017/je5.0.1-64

Benchmarks using both Fortran and C:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-fflto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-align array32byte -ljemalloc -L/home/cpu2017/je5.0.1-64

Benchmarks using both C and C++:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-fflto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc -L/home/cpu2017/je5.0.1-64

Benchmarks using Fortran, C, and C++:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-fflto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-align array32byte -ljemalloc -L/home/cpu2017/je5.0.1-64

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017(flags/Intel-ic2021-official-linux64_revA.2021-12-22.html
http://www.spec.org/cpu2017(flags/Cisco-Platform-Settings-V1.0-ICX-revl.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017(flags/Intel-ic2021-official-linux64_revA.2021-12-22.xml
http://www.spec.org/cpu2017(flags/Cisco-Platform-Settings-V1.0-ICX-revl.xml
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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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