Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Gold 6354, 3.00GHz)

SPEC CPU®2017 Integer Rate Result
Copyright 2017-2022 Standard Performance Evaluation Corporation

Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Gold 6354, 3.00GHz)

SPECrate®2017_int_base = 311
SPECrate®2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Dec-2021
Hardware Availability: Sep-2021
Software Availability: Sep-2021

Hardware
CPU Name: Intel Xeon Gold 6354
Max MHz: 3600
Nominal: 3000
Enabled: 36 cores, 2 chips, 2 threads/core
Orderable: 1,2 Chips
Cache L1: 32 KB I + 48 KB D on chip per core
L2: 1.25 MB I+D on chip per core
L3: 39 MB I+D on chip per chip
Other: None
Memory: 2 TB (32 x 64 GB 2Rx4 PC4-3200AA-R)
Storage: 1 x 240 GB M.2 SSD SATA
Other: None

Software
OS: SUSE Linux Enterprise Server 15 SP3
5.3.18-57-default
Compiler: C/C++ Version 2021.4.0 of Intel oneAPI DPC++/C++
Compiler Build 20210924 for Linux;
Fortran: Version 2021.4.0 of Intel Fortran
Compiler
Classic Build 20210910 for Linux;
Parallel: No
Firmware: Version 5.0.1d released Aug-2021
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: None
Power Management: BIOS and OS set to prefer performance at the cost of additional power usage

Copies
500.perlbench_r  72
502.gcc_r  72
505.mcf_r  72
520.omnetpp_r  72
523.xalancmk_r  72
525.x264_r  72
531.deepsjeng_r  72
541.leela_r  72
548.exchange2_r  72
557.xz_r  72

SPECrate®2017_int_base (311)
SPEC CPU®2017 Integer Rate Result
Copyright 2017-2022 Standard Performance Evaluation Corporation

Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Gold 6354, 3.00GHz)

SPECrate®2017_int_base = 311
SPECrate®2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>72</td>
<td>544</td>
<td>211</td>
<td>543</td>
<td>211</td>
<td>543</td>
<td>211</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>72</td>
<td>393</td>
<td>259</td>
<td>394</td>
<td>259</td>
<td>395</td>
<td>258</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>72</td>
<td>220</td>
<td>529</td>
<td>219</td>
<td>532</td>
<td>219</td>
<td>532</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>72</td>
<td>482</td>
<td>196</td>
<td>478</td>
<td>198</td>
<td>478</td>
<td>198</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>72</td>
<td>189</td>
<td>403</td>
<td>188</td>
<td>404</td>
<td>188</td>
<td>404</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>525.x264_r</td>
<td>72</td>
<td>198</td>
<td>636</td>
<td>198</td>
<td>638</td>
<td>197</td>
<td>639</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>72</td>
<td>347</td>
<td>238</td>
<td>347</td>
<td>238</td>
<td>347</td>
<td>238</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>541.leela_r</td>
<td>72</td>
<td>521</td>
<td>229</td>
<td>521</td>
<td>229</td>
<td>520</td>
<td>229</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>72</td>
<td>305</td>
<td>618</td>
<td>305</td>
<td>618</td>
<td>305</td>
<td>619</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>557.xz_r</td>
<td>72</td>
<td>455</td>
<td>171</td>
<td>456</td>
<td>171</td>
<td>455</td>
<td>171</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH =
"/home/intel/tbb/2021.4.0/env/../lib/intel64/gcc4.8:/home/intel/mpi/2021
.4.0/libfabric/lib:/home/intel/mpi/2021.4.0/lib/release:/home/intel/mp
i/2021.4.0/lib:/home/intel/compiler/2021.4.0/linux/compiler/lib/intel64
_lin:/home/intel/compiler/2021.4.0/linux/lib:/home/intel/clck/2021.4.0/l
ib/intel64:/home/cpu2017/je5.0.1-32"
MALLOC_CONF = "retain:true"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default

(Continued on next page)
Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Gold 6354, 3.00GHz)

SPEC CPU®2017 Integer Rate Result
Copyright 2017-2022 Standard Performance Evaluation Corporation

SPECrate®2017_int_base = 311
SPECrate®2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Dec-2021
Tested by: Cisco Systems
Hardware Availability: Sep-2021
Software Availability: Sep-2021

General Notes (Continued)

Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDC Sparing set to Disabled
Patrol Scrub set to Disabled
Processor C6 Report set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d
running on perf-blade1 Thu Dec 23 07:58:53 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6354 CPU @ 3.00GHz
  2 "physical id"s (chips)
  72 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 18
siblings : 36
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17

From lscpu from util-linux 2.36.2:
Architecture:          x86_64
CPU op-mode(s):        32-bit, 64-bit

(Continued on next page)
Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Gold 6354, 3.00GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Dec-2021
Hardware Availability: Sep-2021
Software Availability: Sep-2021

SPECrate®2017_int_base = 311
SPECrate®2017_int_peak = Not Run

Platform Notes (Continued)

Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 72
On-line CPU(s) list: 0-71
Thread(s) per core: 2
Core(s) per socket: 18
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Gold 6354 CPU @ 3.00GHz
Stepping: 6
CPU MHz: 3528.506
CPU max MHz: 3600.0000
CPU min MHz: 800.0000
BogoMIPS: 6000.00
Virtualization: VT-x
L1d cache: 1.7 MiB
L1i cache: 1.1 MiB
L2 cache: 45 MiB
L3 cache: 78 MiB
NUMA node0 CPU(s): 0-8,36-44
NUMA node1 CPU(s): 9-17,45-53
NUMA node2 CPU(s): 18-26,54-62
NUMA node3 CPU(s): 27-35,63-71
Vulnerability Itlb multihit: Not affected
Vulnerability L1tf: Not affected
Vulnerability Mds: Not affected
Vulnerability Meltdown: Not affected
Vulnerability Spec store bypass: Mitigation; Speculative Store Bypass disabled via prctl and seccomp
Vulnerability Spectre v1: Mitigation; usercopy/swapgs barriers and __user pointer sanitization
Vulnerability Spectre v2: Mitigation; Enhanced IBRS, IBPB conditional, RSB filling
Vulnerability Srbds: Not affected
Vulnerability Tsx async abort: Not affected
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdx86 pmtdesc tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc rcu轮流 perfmonitor pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invpcid_single ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vmx flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb

(Continued on next page)
Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Gold 6354, 3.00GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Dec-2021
Hardware Availability: Sep-2021
Software Availability: Sep-2021

Platform Notes (Continued)

intel_pt axv512cd sha_ni axv512bw axv512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc
cqm_occup_llc cqm_mbm_total cqm_mbm_local split_lock_detect wbnoinvd dtherm ida arat
pln pts hwp hwp_act_window hwp_epp hwp_pkg_req axv512vbmi umip pku ospke
axv512_vbmi2 gfn1 vaes vpclmulqdq avx512_vnni avx512_bitalg tme avx512_vpopcntdq
la57 rdpid fsrm md_clear pconfig flush_l1d arch_capabilities

From lscpu --cache:
NAME ONE-SIZE ALL-SIZE WAYS TYPE LEVEL SETS PHYS-LINE COHERENCY-SIZE
L1d 48K 1.7M 12 Data 1 64 1 64
L1i 32K 1.1M 8 Instruction 1 64 1 64
L2 1.3M 45M 20 Unified 2 1024 1 64
L3 39M 78M 12 Unified 3 53248 1 64

/proc/cpuinfo cache data
cache size: 39936 KB

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 4 nodes (0-3)
note 0 cpus: 0 1 2 3 4 5 6 7 8 36 37 38 39 40 41 42 43 44
node 0 size: 515685 MB
node 0 free: 515339 MB
node 1 cpus: 9 10 11 12 13 14 15 16 17 45 46 47 48 49 50 51 52 53
node 1 size: 516091 MB
node 1 free: 515736 MB
node 2 cpus: 18 19 20 21 22 23 24 25 26 54 55 56 57 58 59 60 61 62
node 2 size: 516091 MB
node 2 free: 515736 MB
node 3 cpus: 27 28 29 30 31 32 33 34 35 63 64 65 66 67 68 69 70 71
node 3 size: 516053 MB
node 3 free: 515738 MB
node distances:
node 0 1 2 3
0: 10 11 20 20
1: 11 10 20 20
2: 20 20 10 11
3: 20 20 11 10

From /proc/meminfo
MemTotal: 2113455436 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*

(Continued on next page)
Platform Notes (Continued)

os-release:
NAME="SLES"
VERSION="15-SP3"
VERSION_ID="15.3"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP3"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp3"

uname -a:
Linux perf-blade1 5.3.18-57-default #1 SMP Wed Apr 28 10:54:41 UTC 2021 (ba3c2e9)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2018-3639 (Speculative Store Bypass): Mitigation: usercopy/swappgs barriers and __user pointer sanitation
CVE-2017-5753 (Spectre variant 1):
CVE-2017-5715 (Spectre variant 2):
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort):

run-level 3 Dec 23 07:58

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda3 xfs 181G 54G 128G 30% /home

From /sys/devices/virtual/dmi/id
Vendor: Cisco Systems Inc
Product: UCSX-210C-M6
Serial: FCH25057AMV

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
## SPEC CPU®2017 Integer Rate Result

**Cisco Systems**
Cisco UCS X210c M6 (Intel Xeon Gold 6354, 3.00GHz)

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>SPECrate®2017_int_base =</td>
<td>311</td>
</tr>
<tr>
<td>SPECrate®2017_int_peak =</td>
<td>Not Run</td>
</tr>
<tr>
<td>Test Date:</td>
<td>Dec-2021</td>
</tr>
<tr>
<td>Hardware Availability:</td>
<td>Sep-2021</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>Sep-2021</td>
</tr>
</tbody>
</table>

### Platform Notes (Continued)

32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200

**BIOS:**
- BIOS Vendor: Cisco Systems, Inc.
- BIOS Version: X210M6.5.0.1.0.0816211754
- BIOS Date: 08/16/2021
- BIOS Revision: 5.22

(End of data from sysinfo program)

### Compiler Version Notes

<table>
<thead>
<tr>
<th>C</th>
<th>500.perlibench_r(base) 502.gcc_r(base) 505.mcf_r(base) 525.x264_r(base) 557.xz_r(base)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.4.0 Build 20210924</td>
<td></td>
</tr>
<tr>
<td>Copyright (C) 1985-2021 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>C++</th>
<th>520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base) 541.leela_r(base)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.4.0 Build 20210924</td>
<td></td>
</tr>
<tr>
<td>Copyright (C) 1985-2021 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Fortran</th>
<th>548.exchange2_r(base)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.4.0 Build 20210910_000000</td>
<td></td>
</tr>
<tr>
<td>Copyright (C) 1985-2021 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
</tbody>
</table>

### Base Compiler Invocation

**C benchmarks:**
- icx

**C++ benchmarks:**
- icpx

(Continued on next page)
# Cisco Systems

Cisco UCS X210c M6 (Intel Xeon Gold 6354, 3.00GHz)

<table>
<thead>
<tr>
<th>CPU2017 License</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Test Date</td>
<td>Dec-2021</td>
</tr>
<tr>
<td>Hardware Availability</td>
<td>Sep-2021</td>
</tr>
<tr>
<td>Software Availability</td>
<td>Sep-2021</td>
</tr>
</tbody>
</table>

## SPECrate®2017_int_base = 311

### Base Compiler Invocation (Continued)

Fortran benchmarks:

`ifort`

## Base Portability Flags

- 500.perlbench_r: `-DSPEC_LP64 -DSPEC_LINUX_X64`
- 502.gcc_r: `-DSPEC_LP64`
- 505.mcf_r: `-DSPEC_LP64`
- 520.omnetpp_r: `-DSPEC_LP64`
- 523.xalancbmk_r: `-DSPEC_LP64 -DSPEC_LINUX`
- 525.x264_r: `-DSPEC_LP64`
- 531.deepsjeng_r: `-DSPEC_LP64`
- 541.leela_r: `-DSPEC_LP64`
- 548.exchange2_r: `-DSPEC_LP64`
- 557.xz_r: `-DSPEC_LP64`

## Base Optimization Flags

### C benchmarks:

```
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc
```

### C++ benchmarks:

```
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc
```

### Fortran benchmarks:

```
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc
```
Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Gold 6354, 3.00GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base = 311</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_int_peak = Not Run</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CPU2017 License: 9019</th>
<th>Test Date: Dec-2021</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor: Cisco Systems</td>
<td>Hardware Availability: Sep-2021</td>
</tr>
<tr>
<td>Tested by: Cisco Systems</td>
<td>Software Availability: Sep-2021</td>
</tr>
</tbody>
</table>

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.0-ICX-revl.xml

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.8 on 2021-12-23 10:58:53-0500.
Originally published on 2022-01-18.