## Cisco Systems

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

### SPEC CPU®2017 Integer Speed Result

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>SPECspeed®2017_int_base</th>
<th>SPECspeed®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>24</td>
<td>8.75</td>
<td>8.77</td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>24</td>
<td>8.75</td>
<td>8.77</td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>1</td>
<td>8.75</td>
<td>8.77</td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>24</td>
<td>8.75</td>
<td>8.77</td>
</tr>
<tr>
<td>623.xalanchmk_s</td>
<td>24</td>
<td>8.75</td>
<td>8.77</td>
</tr>
<tr>
<td>625.x264_s</td>
<td>24</td>
<td>8.75</td>
<td>8.77</td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>1</td>
<td>8.75</td>
<td>8.77</td>
</tr>
<tr>
<td>641.leela_s</td>
<td>24</td>
<td>8.75</td>
<td>8.77</td>
</tr>
<tr>
<td>648.exchange2_s</td>
<td>24</td>
<td>8.75</td>
<td>8.77</td>
</tr>
<tr>
<td>657.xz_s</td>
<td>24</td>
<td>8.75</td>
<td>8.77</td>
</tr>
</tbody>
</table>

### Hardware

**CPU Name:** AMD EPYC 7352  
**Max MHz:** 3200  
**Nominal:** 2300  
**Enabled:** 24 cores, 1 chip, 2 threads/core  
**Orderable:** 1 chips  
**Cache L1:** 32 KB I + 32 KB D on chip per core  
**L2:** 512 KB I+D on chip per core  
**L3:** 128 MB I+D on chip per chip, 16 MB shared / 3 cores  
**Other:** None  
**Memory:** 1 TB (8 x 128 GB 4Rx4 PC4-3200V-L)  
**Storage:** 1 x 960 GB M.2 SSD SATA  
**Other:** None

### Software

**OS:** SUSE Linux Enterprise Server 15 SP3 (x86_64)  
**Compiler:** C/C++/Fortran: Version 3.0.0 of AOCC  
**Parallel:** Yes  
**Firmware:** Version 4.2.1c released Aug-2021  
**File System:** xfs  
**System State:** Run level 3 (multi-user)  
**Base Pointers:** 64-bit  
**Peak Pointers:** 64-bit  
**Other:** jemalloc: jemalloc memory allocator library v5.1.0  
**Power Management:** BIOS and OS set to prefer performance at the cost of additional power usage
Cisco Systems
Cisco UCS C225 M6 (AMD EPYC 7352 24-Core)

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>24</td>
<td>371</td>
<td>4.78</td>
<td>374</td>
<td>4.74</td>
<td>372</td>
<td>4.78</td>
<td>24</td>
<td>371</td>
<td>4.78</td>
<td>374</td>
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<tr>
<td>602.gcc_s</td>
<td>24</td>
<td>429</td>
<td>9.28</td>
<td>428</td>
<td>9.30</td>
<td>428</td>
<td>9.30</td>
<td>24</td>
<td>429</td>
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<td>428</td>
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<tr>
<td>605.mcf_s</td>
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<td>316</td>
<td>14.9</td>
<td>316</td>
<td>14.9</td>
<td>318</td>
<td>14.9</td>
<td>1</td>
<td>315</td>
<td>15.0</td>
<td>316</td>
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<tr>
<td>620.omnetpp_s</td>
<td>24</td>
<td>338</td>
<td>4.83</td>
<td>336</td>
<td>4.85</td>
<td>337</td>
<td>4.84</td>
<td>24</td>
<td>338</td>
<td>4.83</td>
<td>336</td>
</tr>
<tr>
<td>623.xalanchmk_s</td>
<td>24</td>
<td>142</td>
<td>9.98</td>
<td>141</td>
<td>10.0</td>
<td>142</td>
<td>9.98</td>
<td>24</td>
<td>142</td>
<td>9.98</td>
<td>141</td>
</tr>
<tr>
<td>625.x264_s</td>
<td>24</td>
<td>135</td>
<td>13.1</td>
<td>137</td>
<td>12.9</td>
<td>135</td>
<td>13.1</td>
<td>1</td>
<td>135</td>
<td>13.1</td>
<td>135</td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>24</td>
<td>299</td>
<td>4.80</td>
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<td>4.80</td>
<td>301</td>
<td>4.76</td>
<td>1</td>
<td>298</td>
<td>4.81</td>
<td>298</td>
</tr>
<tr>
<td>641.leela_s</td>
<td>24</td>
<td>411</td>
<td>4.15</td>
<td>411</td>
<td>4.15</td>
<td>411</td>
<td>4.15</td>
<td>24</td>
<td>411</td>
<td>4.15</td>
<td>411</td>
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<tr>
<td>648.exchange2_s</td>
<td>24</td>
<td>176</td>
<td>16.7</td>
<td>176</td>
<td>16.7</td>
<td>176</td>
<td>16.7</td>
<td>1</td>
<td>176</td>
<td>16.8</td>
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<tr>
<td>657.xz_s</td>
<td>24</td>
<td>326</td>
<td>19.0</td>
<td>325</td>
<td>19.0</td>
<td>325</td>
<td>19.0</td>
<td>24</td>
<td>325</td>
<td>19.0</td>
<td>325</td>
</tr>
</tbody>
</table>

SPECspeed®2017_int_base = 8.75
SPECspeed®2017_int_peak = 8.77

Compiler Notes

The AMD64 AOCC Compiler Suite is available at http://developer.amd.com/amd-aocc/

Submit Notes

The config file option 'submit' was used.
'numactl' was used to bind copies to the cores.
See the configuration file for details.

Operating System Notes

'ulimit -s unlimited' was used to set environment stack size limit
'ulimit -l 2097152' was used to set environment locked pages in memory limit
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

To limit dirty cache to 8% of memory, 'sysctl -w vm.dirty_ratio=8' run as root.
To limit swap usage to minimum necessary, 'sysctl -w vm.swappiness=1' run as root.
To free node-local memory and avoid remote memory usage,
'sysctl -w vm.zone_reclaim_mode=1' run as root.
To clear filesystem caches, 'sync; sysctl -w vm.drop_caches=3' run as root.
To disable address space layout randomization (ASLR) to reduce run-to-run variability, 'sysctl -w kernel.randomize_va_space=0' run as root.

To enable Transparent Hugepages (THP) for all allocations,
Cisco Systems
Cisco UCS C225 M6 (AMD EPYC 7352 24-Core)

SPECcpu2017 int peak = 8.77
SPECcpu2017 int base = 8.75

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Operating System Notes (Continued)

'echo always > /sys/kernel/mm/transparent_hugepage/enabled' and
'echo always > /sys/kernel/mm/transparent_hugepage/defrag' run as root.

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
GOMP_CPU_AFFINITY = "0-47"
LD_LIBRARY_PATH = "/home/cpu2017/amd_speed_aocc300_milan_B_lib/lib;/home/cpu2017/amd_speed_aocc300_milan_B_lib/lib32:"
MALLOCP_CONF = "retain:true"
OMP_DYNAMIC = "false"
OMP_SCHEDULE = "static"
OMP_STACKSIZE = "592M"
OMP_THREAD_LIMIT = "48"

Environment variables set by runcpu during the 605.mcf_s peak run:
GOMP_CPU_AFFINITY = "0"

Environment variables set by runcpu during the 625.x264_s peak run:
GOMP_CPU_AFFINITY = "0"

Environment variables set by runcpu during the 631.deepsjeng_s peak run:
GOMP_CPU_AFFINITY = "0"

Environment variables set by runcpu during the 648.exchange2_s peak run:
GOMP_CPU_AFFINITY = "0"

Environment variables set by runcpu during the 657.xz_s peak run:
GOMP_CPU_AFFINITY = "0-23"

General Notes

Binaries were compiled on a system with 2x AMD EPYC 7742 CPU + 1TiB Memory using openSUSE 15.2

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc: configured and built with GCC v4.8.2 in RHEL 7.4 (No options specified)
jemalloc 5.1.0 is available here:
https://github.com/jemalloc/jemalloc/releases/download/5.1.0/jemalloc-5.1.0.tar.bz2
## Platform Notes

SMT Mode set to Auto  
NUMA nodes per socket set to NPS1  
ACPI SRAT L3 Cache As NUMA Domain set to Enabled  
DRAM Scrub Time set to Disabled  
Determinism Slider set to Power  
L1 Stream HW Prefetcher set to Enabled  
APBDIS set to 1  

Sysinfo program /home/cpu2017/bin/sysinfo  
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16aca6b64d  
r蕃ng on localhost Mon Dec  6 07:01:14 2021  

SUT (System Under Test) info as seen by some common utilities.  
For more information on this section, see  
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

<table>
<thead>
<tr>
<th>From /proc/cpuinfo</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>model name</td>
<td>AMD EPYC 7352 24-Core Processor</td>
</tr>
<tr>
<td>1 &quot;physical id&quot;s (chips)</td>
<td>48 &quot;processors&quot;</td>
</tr>
<tr>
<td>cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)</td>
<td></td>
</tr>
<tr>
<td>cpu cores</td>
<td>24</td>
</tr>
<tr>
<td>siblings</td>
<td>48</td>
</tr>
<tr>
<td>physical 0: cores</td>
<td>0 1 2 4 5 6 8 9 10 12 13 14 16 17 18 20 21 22 24 25 26 28 29 30</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>From lscpu from util-linux 2.36.2:</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Architecture</td>
<td>x86_64</td>
</tr>
<tr>
<td>CPU op-mode(s):</td>
<td>32-bit, 64-bit</td>
</tr>
<tr>
<td>Byte Order:</td>
<td>Little Endian</td>
</tr>
<tr>
<td>Address sizes:</td>
<td>43 bits physical, 48 bits virtual</td>
</tr>
<tr>
<td>CPU(s):</td>
<td>48</td>
</tr>
<tr>
<td>On-line CPU(s) list:</td>
<td>0-47</td>
</tr>
<tr>
<td>Thread(s) per core:</td>
<td>2</td>
</tr>
<tr>
<td>Core(s) per socket:</td>
<td>24</td>
</tr>
<tr>
<td>Socket(s):</td>
<td>1</td>
</tr>
<tr>
<td>NUMA node(s):</td>
<td>4</td>
</tr>
<tr>
<td>Vendor ID:</td>
<td>AuthenticAMD</td>
</tr>
<tr>
<td>CPU family:</td>
<td>23</td>
</tr>
<tr>
<td>Model:</td>
<td>49</td>
</tr>
<tr>
<td>Model name:</td>
<td>AMD EPYC 7352 24-Core Processor</td>
</tr>
<tr>
<td>Stepping:</td>
<td>0</td>
</tr>
<tr>
<td>Frequency boost:</td>
<td>enabled</td>
</tr>
<tr>
<td>CPU MHz:</td>
<td>1496.624</td>
</tr>
<tr>
<td>CPU max MHz:</td>
<td>2300.0000</td>
</tr>
<tr>
<td>CPU min MHz:</td>
<td>1500.0000</td>
</tr>
<tr>
<td>BogoMIPS:</td>
<td>4591.66</td>
</tr>
</tbody>
</table>

(Continued on next page)
Cisco Systems
Cisco UCS C225 M6 (AMD EPYC 7352 24-Core)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Dec-2021
Tested by: Cisco Systems
Hardware Availability: Jun-2021
Software Availability: Jun-2021

SPECspeed®2017_int_base = 8.75
SPECspeed®2017_int_peak = 8.77

Platform Notes (Continued)

Virtualization: AMD-V
L1d cache: 768 KiB
L1i cache: 768 KiB
L2 cache: 12 MiB
L3 cache: 128 MiB
NUMA node0 CPU(s): 0-5, 24-29
NUMA node1 CPU(s): 6-11, 30-35
NUMA node2 CPU(s): 12-17, 36-41
NUMA node3 CPU(s): 18-23, 42-47
Vulnerability Itlb multihit: Not affected
Vulnerability L1t: Not affected
Vulnerability Mds: Not affected
Vulnerability Meltdown: Not affected
Vulnerability Spec store bypass: Mitigation; Speculative Store Bypass disabled via prctl and seccomp
Vulnerability Spectre v1: Mitigation; usercopy/swapgs barriers and __user pointer sanitation
Vulnerability Spectre v2: Mitigation; Full AMD retpoline, IBPF conditional, IBRS_FW, STIBF conditional, RSB filling
Vulnerability Srbds: Not affected
Vulnerability Tsx async abort: Not affected

From lscpu --cache:
NAME ONE-SIZE ALL-SIZE WAYS TYPE LEVEL SETS PHY-LINE COHERENCY-SIZE
L1d 32K 768K 8 Data 1 64 1 64
L1i 32K 768K 8 Instruction 1 64 1 64
L2 512K 12M 8 Unified 2 1024 1 64
L3 16M 128M 16 Unified 3 16384 1 64

/proc/cpuinfo cache data
cache size : 512 KB

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 4 nodes (0-3)

(Continued on next page)
Cisco Systems

Cisco UCS C225 M6 (AMD EPYC 7352 24-Core)

<table>
<thead>
<tr>
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<td>Test Date: Dec-2021</td>
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<td>Hardware Availability: Jun-2021</td>
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<td>Tested by: Cisco Systems</td>
<td>Software Availability: Jun-2021</td>
</tr>
</tbody>
</table>

Platform Notes (Continued)

```
node 0 cpus: 0 1 2 3 4 5 24 25 26 27 28 29
node 0 size: 257860 MB
node 0 free: 257522 MB
node 1 cpus: 6 7 8 9 10 11 30 31 32 33 34 35
node 1 size: 258043 MB
node 1 free: 257782 MB
node 2 cpus: 12 13 14 15 16 17 36 37 38 39 40 41
node 2 size: 258043 MB
node 2 free: 257433 MB
node 3 cpus: 18 19 20 21 22 23 42 43 44 45 46 47
node 3 size: 257997 MB
node 3 free: 257691 MB
node distances:
  node 0  1  2  3
  0:  10 12 12 12
  1:  12 10 12 12
  2:  12 12 10 12
  3:  12 12 12 10

From /proc/meminfo
  MemTotal: 1056712372 kB
  HugePages_Total: 0
  Hugepagesize: 2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has ondemand

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15-SP3"
    VERSION_ID="15.3"
    PRETTY_NAME="SUSE Linux Enterprise Server 15 SP3"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15:sp3"

uname -a:
  Linux localhost 5.3.18-57-default #1 SMP Wed Apr 28 10:54:41 UTC 2021 (ba3c2e9) x86_64
  x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
```

(Continued on next page)
Cisco UCS C225 M6 (AMD EPYC 7352 24-Core)

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<tr>
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CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems

**Platform Notes (Continued)**

<table>
<thead>
<tr>
<th>CVE-2017-5754 (Meltdown):</th>
<th>Not affected</th>
</tr>
</thead>
<tbody>
<tr>
<td>CVE-2018-3639 (Speculative Store Bypass):</td>
<td>Mitigation: Speculative Store Bypass disabled via prctl and seccomp</td>
</tr>
<tr>
<td>CVE-2017-5753 (Spectre variant 1):</td>
<td>Mitigation: usercopy/swapgs barriers and __user pointer sanitization</td>
</tr>
<tr>
<td>CVE-2017-5715 (Spectre variant 2):</td>
<td>Mitigation: Full AMD retpoline, IBPB: conditional, IBRS_FW, STIBP: conditional, RSB filling</td>
</tr>
<tr>
<td>CVE-2020-0543 (Special Register Buffer Data Sampling):</td>
<td>Not affected</td>
</tr>
<tr>
<td>CVE-2019-11135 (TSX Asynchronous Abort):</td>
<td>Not affected</td>
</tr>
</tbody>
</table>

runtime 3 Dec 6 07:00

SPEC is set to: /home/cpu2017

```
Filesystem  Type  Size  Used  Avail  Use% Mounted on
/dev/sda3    xfs   557G   11G  546G   2%  /
```

From /sys/devices/virtual/dmi/id

Vendor: Cisco Systems Inc
Product: To

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:

8x 0xCE00 M386AAG40AM3-CWE 128 GB 4 rank 3200

BIOS:

<table>
<thead>
<tr>
<th>BIOS Vendor: Cisco Systems Inc</th>
</tr>
</thead>
<tbody>
<tr>
<td>BIOS Version: C225M6.4.2.1c.0.0806211349</td>
</tr>
<tr>
<td>BIOS Date: 08/06/2021</td>
</tr>
<tr>
<td>BIOS Revision: 5.14</td>
</tr>
</tbody>
</table>

(End of data from sysinfo program)

**Compiler Version Notes**

```
C | 600.perlbench_s(base, peak) 602.gcc_s(base, peak) 605.mcf_s(base, peak) 625.x264_s(base, peak) 657.xz_s(base, peak)
```

AMD clang version 12.0.0 (CLANG: AOCC_3.0.0-Build#78 2020_12_10) (based on LLVM Mirror.Version.12.0.0)
Cisco Systems
Cisco UCS C225 M6 (AMD EPYC 7352 24-Core)

SPECspec®2017_int_base = 8.75
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Dec-2021
Hardware Availability: Jun-2021

Tested by: Cisco Systems
Software Availability: Jun-2021

Compiler Version Notes (Continued)

Target: x86_64-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.0.0/bin

------------------------------------------------------------------------------
==============================================================================
C++     | 620.omnetpp_s(base, peak) 623.xalancbmk_s(base, peak)
        | 631.deepsjeng_s(base, peak) 641.leela_s(base, peak)
------------------------------------------------------------------------------
AMD clang version 12.0.0 (CLANG: AOCC_3.0.0-Build#78 2020_12_10) (based on
LLVM Mirror.Version.12.0.0)
Target: x86_64-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.0.0/bin

------------------------------------------------------------------------------
==============================================================================
Fortran | 648.exchange2_s(base, peak)
------------------------------------------------------------------------------
AMD clang version 12.0.0 (CLANG: AOCC_3.0.0-Build#78 2020_12_10) (based on
LLVM Mirror.Version.12.0.0)
Target: x86_64-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.0.0/bin

Base Compiler Invocation

C benchmarks:
clang

C++ benchmarks:
clang++

Fortran benchmarks:
flang

Base Portability Flags

600.perlbench_s: -DSPEC_LINUX_X64 -DSPEC_LP64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64

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Base Portability Flags (Continued)

623.xalancbmk_s: -DSPEC_LINUX -DSPEC_LP64
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-m64 -mno-adx -mno-sse4a -Wl,-allow-multiple-definition
-Wl,-mlvm -Wl,-enable-licm-vrp -Wl,-mllvvm -Wl,-region-vectorize
-Wl,-mllvvm -Wl,-function-specialize
-Wl,-mllvvm -Wl,-align-all-nofallthru-blocks=6
-Wl,-mllvvm -Wl,-reduce-array-computations=3 -O3 -march=znver3
-fveclib=AMDLIBM -ffast-math -flto -fstruct-layout=5
-mllvvm -unroll-threshold=50 -mllvvm -inline-threshold=1000
-fremap-arrays -mllvvm -function-specialize -flv-function-specialization
-mllvvm -enable-gvn-hoist -mllvvm -global-vectorize-slp=true
-mllvvm -enable-licm-vrp -mllvvm -reduce-array-computations=3 -z muldefs
-DSPEC_OPENMP -fopenmp -fopenmp=libomp -lomp -lamdlibm -ljemalloc
-lflang -lflangrti

C++ benchmarks:
-m64 -std=c++98 -mno-adx -mno-sse4a
-Wl,-mllvvm -Wl,-do-block-reorder=aggressive
-Wl,-mllvvm -Wl,-region-vectorize -Wl,-mllvvm -Wl,-function-specialize
-Wl,-mllvvm -Wl,-align-all-nofallthru-blocks=6
-Wl,-mllvvm -Wl,-reduce-array-computations=3 -O3 -march=znver3
-fveclib=AMDLIBM -ffast-math -flto -mllvvm -enable-partial-unswitch
-mllvvm -unroll-threshold=100 -finline-aggressive
-flv-function-specialization -mllvvm -loop-unswitch-threshold=200000
-mllvvm -reroll-loops -mllvvm -aggressive-loop-unswitch
-mllvvm -extra-vectorizer-passes -mllvvm -reduce-array-computations=3
-mllvvm -global-vectorize-slp=true -mllvvm -convert-pow-exp-to-int=false
-z muldefs -mllvvm -do-block-reorder=aggressive
-fvirtual-function-elimination -fvisibility=hidden -DSPEC_OPENMP
-fopenmp -fopenmp=libomp -lomp -lamdlibm -ljemalloc -lflang
-lflangrti

Fortran benchmarks:
-m64 -mno-adx -mno-sse4a -Wl,-mllvvm -Wl,-inline-recursion=4
-Wl,-mllvvm -Wl,-lsr-in-nested-loop -Wl,-mllvvm -Wl,-enable-iv-split
-Wl,-mllvvm -Wl,-region-vectorize -Wl,-mllvvm -Wl,-function-specialize

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## SPEC CPU®2017 Integer Speed Result

**Cisco Systems**

Cisco UCS C225 M6 (AMD EPYC 7352 24-Core)

| SPECspeed®2017_int_base = 8.75 |
| SPECspeed®2017_int_peak = 8.77 |

| CPU2017 License: 9019 | Test Date: Dec-2021 |
| Test Sponsor: Cisco Systems | Hardware Availability: Jun-2021 |
| Tested by: Cisco Systems | Software Availability: Jun-2021 |

### Base Optimization Flags (Continued)

- Fortran benchmarks (continued):
  - `-Wl, -mllvm -Wl, -align-all-nofallthru-blocks=6`
  - `-Wl, -mllvm -Wl, -reduce-array-computations=3 -O3 -march=znver3`
  - `-fveclib=AMDLIBM -ffast-math -flto -z muldefs`
  - `-mllvm -unroll-aggressive -mllvm -unroll-threshold=150 -DSPEC_OPENMP`
  - `-fopenmp -fopenmp=libomp -lomp -lamdlibm -ljemalloc -lflang -lflangrti`

### Base Other Flags

- C benchmarks:
  - `-Wno-unused-command-line-argument -Wno-return-type`

- C++ benchmarks:
  - `-Wno-unused-command-line-argument -Wno-return-type`

- Fortran benchmarks:
  - `-Wno-return-type`

### Peak Compiler Invocation

- C benchmarks:
  - `clang`

- C++ benchmarks:
  - `clang++`

- Fortran benchmarks:
  - `flang`

### Peak Portability Flags

Same as Base Portability Flags
Cisco Systems
Cisco UCS C225 M6 (AMD EPYC 7352 24-Core)

| SPECspeed®2017_int_base = 8.75 |
| SPECspeed®2017_int_peak = 8.77 |

CPU2017 License: 9019
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Tested by: Cisco Systems
Hardware Availability: Jun-2021
Software Availability: Jun-2021

Peak Optimization Flags

C benchmarks:

600.perlbench_s: basepeak = yes

602.gcc_s: basepeak = yes

605.mcf_s: -m64 -mno-adx -mno-sse4a -Wl,-allow-multiple-definition
-We -ml1v -Wl,-enable-licm-vrp
-We -ml1v -Wl,-function-specialize
-We -ml1v -Wl,-align-all-nofallthru-blocks=6
-We -ml1v -Wl,-reduce-array-computations=3 -Ofast
-march=znver3 -fveclib=AMDLIBM -ffast-math -flto
-fstruct-layout=5 -ml1v -unroll-threshold=50
-fremap-arrays -flv-function-specialization
-ml1v -inline-threshold=1000 -ml1v -enable-gvn-hoist
-ml1v -global-vectorize-slp=true
-ml1v -function-specialize -ml1v -enable-licm-vrp
-ml1v -reduce-array-computations=3 -DSPEC_OPENMP -fopenmp
-fopenmp=libomp -lomp -lamdllbm -ljemalloc -lflang

625.x264_s: Same as 605.mcf_s

657.xz_s: Same as 605.mcf_s

C++ benchmarks:

620.omnetpp_s: basepeak = yes

623.xalancbmk_s: basepeak = yes

631.deepsjeng_s: -m64 -std=c++98 -mno-adx -mno-sse4a
-We -ml1v -Wl,-do-block-reorder=aggressive
-We -ml1v -Wl,-function-specialize
-We -ml1v -Wl,-align-all-nofallthru-blocks=6
-We -ml1v -Wl,-reduce-array-computations=3 -Ofast
-march=znver3 -fveclib=AMDLIBM -ffast-math -flto
-finline-aggressive -ml1v -unroll-threshold=100
-flv-function-specialization -ml1v -enable-licm-vrp
-ml1v -reroll-loops -ml1v -aggressive-loop-unswitch
-ml1v -reduce-array-computations=3
-ml1v -global-vectorize-slp=true
-ml1v -do-block-reorder=aggressive
-fvirtual-function-elimination -fvisibility=hidden
-DSPEC_OPENMP -fopenmp -fopenmp=libomp -lomp -lamdllbm
-ljemalloc -lflang

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Cisco Systems
Cisco UCS C225 M6 (AMD EPYC 7352 24-Core)

<table>
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</tbody>
</table>

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Dec-2021
Hardware Availability: Jun-2021
Software Availability: Jun-2021

Peak Optimization Flags (Continued)

641.leela_s: basepeak = yes

Fortran benchmarks:
- m64 -mno-adx -mno-sse4a -W1, -ml1vm -W1, -inline-recursion=4
- W1, -ml1vm -W1, -lsr-in-nested-loop -W1, -ml1vm -W1, -enable-iv-split
- W1, -ml1vm -W1, -function-specialize
- W1, -ml1vm -W1, -align-all-nofallthru-blocks=6
- W1, -ml1vm -W1, -reduce-array-computations=3 -O3 -march=znver3
- fvecLib=AMDLIBM -ffast-math -flto -ml1vm -unroll-aggressive
- ml1vm -unroll-threshold=150 -DSPEC_OPENMP -fopenmp -fopenmp=libomp
- lomp -lamdlibm -ljemalloc -flang

Peak Other Flags

C benchmarks:
-Wno-unused-command-line-argument -Wno-return-type

C++ benchmarks:
-Wno-unused-command-line-argument -Wno-return-type

Fortran benchmarks:
-Wno-return-type

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:

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