Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Gold 6346, 3.10GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base</th>
<th>321</th>
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<tbody>
<tr>
<td>SPECrate®2017_fp_peak</td>
<td>Not Run</td>
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CPU2017 License: 9019  Test Date: Dec-2021
Test Sponsor: Cisco Systems  Hardware Availability: Sep-2021
Tested by: Cisco Systems  Software Availability: Sep-2021

### Copies

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<thead>
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<th>SPECrate®2017_fp_base (321)</th>
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<tr>
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<td>503.bwaves_r</td>
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<tr>
<td>507.cactuBSSN_r</td>
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<tr>
<td>508.namd_r</td>
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<tr>
<td>510.parest_r</td>
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<tr>
<td>511.povray_r</td>
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<tr>
<td>521.wrf_r</td>
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<td>526.blender_r</td>
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<tr>
<td>527.cam4_r</td>
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<td>538.imagick_r</td>
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<td>544.nab_r</td>
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<tr>
<td>549.fotonik3d_r</td>
</tr>
<tr>
<td>554.roms_r</td>
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</table>

### Hardware

**CPU Name:** Intel Xeon Gold 6346
**Max MHz:** 3600
**Nominal:** 3100
**Enabled:** 32 cores, 2 chips, 2 threads/core
**Orderable:** 1,2 Chips
**Cache L1:** 32 KB I + 48 KB D on chip per core
**L2:** 1.25 MB I+D on chip per core
**L3:** 36 MB I+D on chip per chip
**Other:** None
**Memory:** 2 TB (32 x 64 GB 2Rx4 PC4-3200AA-R)
**Storage:** 1 x 240 GB M.2 SSD SATA
**Other:** None

### Software

**OS:** SUSE Linux Enterprise Server 15 SP2
**Version:** 5.3.18-22-default

**Compiler:** C/C++: Version 2021.4.0 of Intel oneAPI DPC++/C++
**Compiler Build:** 20210924 for Linux;
**Fortran:** Version 2021.4.0 of Intel Fortran
**Compiler:** Classic Build 20210910 for Linux;

**Parallel:** No
**Firmware:** Version 5.0.1d released Aug-2021
**File System:** btrfs
**System State:** Run level 3 (multi-user)
**Base Pointers:** 64-bit
**Peak Pointers:** Not Applicable
**Other:** jemalloc memory allocator V5.0.1
**Power Management:** BIOS and OS set to prefer performance at the cost of additional power usage
### Cisco Systems
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**Hardware Availability:** Sep-2021  
**Software Availability:** Sep-2021

### Results Table

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</tr>
</tbody>
</table>

**SPECrate®2017_fp_base = 321**  
**SPECrate®2017_fp_peak = Not Run**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes
Environment variables set by runcpu before the start of the run:

```bash
LD_LIBRARY_PATH = "/home/intel/tbb/2021.4.0/env/../lib/intel64/gcc4.8:/home/intel/mpi/2021
.4.0/libfabric/lib:/home/intel/mpi/2021.4.0/lib/release:/home/intel/mp
i/2021.4.0/lib:/home/intel/compiler/2021.4.0/lib/gcc/intel64
_lin:/home/intel/compiler/2021.4.0/lib/intel/gcc/2021.4.0/lib/int
el64:/home/cpu2017/je5.0.1-32"
MALLOC_CONF = "retain:true"
```
Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Gold 6346, 3.10GHz)

SPEC CPU®2017 Floating Point Rate Result
Copyright 2017-2021 Standard Performance Evaluation Corporation

SPECrate®2017_fp_base = 321
SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

General Notes

Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM
memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
    sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
    numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDDC Sparing set to Disabled
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d
running on perf-blade3 Wed Dec 1 13:59:51 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
    model name : Intel(R) Xeon(R) Gold 6346 CPU @ 3.10GHz
        2 "physical id"s (chips)
        64 "processors"
core, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 16
siblings : 32
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

Page 3
## Platform Notes (Continued)

### Physical 1: Cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From `lscpu` from `util-linux 2.33.1`:

- **Architecture:** x86_64
- **CPU op-mode(s):** 32-bit, 64-bit
- **Byte Order:** Little Endian
- **Address sizes:** 46 bits physical, 57 bits virtual
- **CPU(s):** 64
- **On-line CPU(s) list:** 0-63
- **Thread(s) per core:** 2
- **Core(s) per socket:** 16
- **Socket(s):** 2
- **NUMA node(s):** 4
- **Vendor ID:** GenuineIntel
- **CPU family:** 6
- **Model:** 106
- **Model name:** Intel(R) Xeon(R) Gold 6346 CPU @ 3.10GHz
- **Stepping:** 6
- **CPU MHz:** 2394.123
- **CPU max MHz:** 3600.0000
- **CPU min MHz:** 800.0000
- **BogoMIPS:** 6200.00
- **Virtualization:** VT-x
- **L1d cache:** 48K
- **L1l cache:** 32K
- **L2 cache:** 1280K
- **L3 cache:** 36864K
- **NUMA node0 CPU(s):** 0-7, 32-39
- **NUMA node1 CPU(s):** 8-15, 40-47
- **NUMA node2 CPU(s):** 16-23, 48-55
- **NUMA node3 CPU(s):** 24-31, 56-63
- **Flags:** fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtrac xtpr pdcm pclid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invpcid_single ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vmmi flexpriority ept vpid ept_ad fsalgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha ni avx512bw avx512vl xsaveopt xsavec xsaveopt xsaves cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local wbinvd dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req avx512vmbmi umip pku ospke avx512v bmi2 gfnf vaes vpclmulqdq avx512_vnni avx512_bitalg tme avx512_vpopcntdq la57 rdrpid md_clear pconfig flush_lid arch_capabilities

/proc/cpuinfo cache data

(Continued on next page)
Platform Notes (Continued)

```
cache size : 36864 KB

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 4 5 6 7 32 33 34 35 36 37 38 39
node 0 size: 515685 MB
node 0 free: 515344 MB
node 1 cpus: 8 9 10 11 12 13 14 15 40 41 42 43 44 45 46 47
node 1 size: 516091 MB
node 1 free: 515840 MB
node 2 cpus: 16 17 18 19 20 21 22 23 48 49 50 51 52 53 54 55
node 2 size: 516091 MB
node 2 free: 515826 MB
node 3 cpus: 24 25 26 27 28 29 30 31 56 57 58 59 60 61 62 63
node 3 size: 516054 MB
node 3 free: 515776 MB
node distances:
node   0   1   2   3
0:  10  11  20  20
1:  11  10  20  20
2:  20  20  10  11
3:  20  20  11  10

From /proc/meminfo
MemTotal:       2113458076 kB
HugePages_Total:       0
Hugepagesize:       2048 kB
/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15-SP2"
    VERSION_ID="15.2"
    PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
  Linux perf-blade3 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba)
  x86_64 x86_64 x86_64 GNU/Linux

(Continued on next page)
Cisco Systems
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SPECrater®2017_fp_base = 321
SPECrater®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2018-3639 (Speculative Store Bypass): Mitigation: usercopy/swapgs barriers and __user pointer sanitization
CVE-2018-5735 (Spectre variant 1): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Dec 1 13:53

SPEC is set to: /home/cpu2017

FILESYSTEM TYPE SIZE USED AVAIL USE% MOUNTED ON
/dev/sda2 btrfs 222G 60G 162G 27% /home

From /sys/devices/virtual/dmi/id
Vendor: Cisco Systems Inc
Product: UCSX-210C-M6
Serial: FCH25057AL5

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200

BIOS:
BIOS Vendor: Cisco Systems, Inc.
BIOS Version: X210M6.5.01d.0.0816211754
BIOS Date: 08/16/2021
BIOS Revision: 5.22

(End of data from sysinfo program)
Compiler Version Notes

==============================================================================
C | 519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)
-----------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.4.0 Build 20210924  
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.
-----------------------------------------------------------------------------

C++ | 508.namd_r(base) 510.parest_r(base)
-----------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.4.0 Build 20210924  
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.
-----------------------------------------------------------------------------

C++, C | 511.povray_r(base) 526.blender_r(base)
-----------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.4.0 Build 20210924  
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.4.0 Build 20210924  
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.
-----------------------------------------------------------------------------

C++, C, Fortran | 507.cactuBSSN_r(base)
-----------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.4.0 Build 20210924  
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
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Copyright (C) 1985-2021 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on  
Intel(R) 64, Version 2021.4.0 Build 20210910_000000  
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.
-----------------------------------------------------------------------------

Fortran | 503.bwaves_r(base) 549.fotonik3d_r(base) 554.roms_r(base)
-----------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on  
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(Continued on next page)
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Test Date: Dec-2021
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Compiler Version Notes (Continued)

==============================================================================
Fortran, C     | 521.wrf_r(base) 527.cam4_r(base)
==============================================================================
Intel (R) Fortran Intel (R) 64 Compiler Classic for applications running on
Intel (R) 64, Version 2021.4.0 Build 20210910_000000
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.
Intel (R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.4.0 Build 20210924
Copyright (C) 1985-2021 Intel Corporation. All rights reserved.
==============================================================================

Base Compiler Invocation

C benchmarks:
icx
C++ benchmarks:
icpx
Fortran benchmarks:
ifort
Benchmarks using both Fortran and C:
ifort icx
Benchmarks using both C and C++:
icpx icx
Benchmarks using Fortran, C, and C++:
icpx icx ifort

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigend-char

(Continued on next page)
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SPECrate®2017_fp_base = 321
SPECrate®2017_fp_peak = Not Run

Test Hardware Availability: Sep-2021
Software Availability: Sep-2021

Base Portability Flags (Continued)

527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-w -std=c11 -m64 -Wl,-z,-muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc -L/home/cpu2017/je5.0.1-64

C++ benchmarks:
-w -m64 -Wl,-z,-muldefs -xCORE-AVX512 -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc -L/home/cpu2017/je5.0.1-64

Fortran benchmarks:
-w -m64 -Wl,-z,-muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
-qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte
-mbranches-within-32B-boundaries -ljemalloc -L/home/cpu2017/je5.0.1-64

Benchmarks using both Fortran and C:
-w -m64 -std=c11 -Wl,-z,-muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-align array32byte -ljemalloc -L/home/cpu2017/je5.0.1-64

Benchmarks using both C and C++:
-w -m64 -std=c11 -Wl,-z,-muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc -L/home/cpu2017/je5.0.1-64

Benchmarks using Fortran, C, and C++:
-w -m64 -std=c11 -Wl,-z,-muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -nostandard-realloc-lhs

(Continued on next page)
**Cisco Systems**
Cisco UCS X210c M6 (Intel Xeon Gold 6346, 3.10GHz)

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**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Dec-2021  
**Hardware Availability:** Sep-2021  
**Software Availability:** Sep-2021

### Base Optimization Flags (Continued)

Benchmarks using Fortran, C, and C++ (continued):
- `-align array32byte`  
- `-ljemalloc`  
- `-L/home/cpu2017/je5.0.1-64`

The flags files that were used to format this result can be browsed at:

You can also download the XML flags sources by saving the following links:

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