## Cisco Systems

Cisco UCS X210c M6 (Intel Xeon Gold 6338N, 2.20GHz)

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<tr>
<th>SPECspeed®2017_int_base</th>
<th>11.8</th>
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<tbody>
<tr>
<td>SPECspeed®2017_int_peak</td>
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</table>

### Software

- **OS:** SUSE Linux Enterprise Server 15 SP2
- **Compiler:** C/C++: Version 2021.4.0 of Intel oneAPI DPC++/C++
- **Firmware:** Version 5.0.1d released Aug-2021
- **System State:** Run level 3 (multi-user)
- **Power Management:** BIOS and OS set to prefer performance at the cost of additional power usage

### Hardware

- **CPU Name:** Intel Xeon Gold 6338N
- **Max MHz:** 3500
- **Nominal:** 2200
- **Enabled:** 64 cores, 2 chips
- **Orderable:** 1.2 Chips
- **Cache L1:** 32 KB I + 48 KB D on chip per core
- **L2:** 1.25 MB I+D on chip per core
- **L3:** 48 MB I+D on chip per chip
- **Memory:** 2 TB (32 x 64 GB 2Rx4 PC4-3200AA-R, running at 2666)
- **Storage:** 1 x 240 GB M.2 SSD SATA
- **Other:** None

### Test Information

- **CPU2017 License:** 9019
- **Test Sponsor:** Cisco Systems
- **Test Date:** Nov-2021
- **Hardware Availability:** Sep-2021
- **Tested by:** Cisco Systems
- **Software Availability:** Sep-2021
Cisco Systems
Cisco UCS X210c M6 (Intel Xeon Gold 6338N, 2.20GHz)

SPEC CPU®2017 Integer Speed Result

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<td>23.7</td>
<td>64</td>
<td>262</td>
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<td>259</td>
</tr>
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</table>

SPECspeed®2017_int_base = 11.8
SPECspeed®2017_int_peak = 12.0

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,scatter"
LD_LIBRARY_PATH = 
"/home/intel/tbb/2021.4.0/env/..lib/intel64/gcc4.8:/home/intel/mpi/2021
.4.0/libfabric/lib:/home/intel/mpi/2021.4.0//lib/release:/home/intel/mp
i/2021.4.0/lib:/home/intel/compiler/2021.4.0/linux/compiler/lib/intel64
_lin:/home/intel/compiler/2021.4.0/linux/lib:/home/intel/clck/2021.4.0/l
ib/intel64:/home/cpu2017/je5.0.1-32"
MALLOCONF = "retain: true"
OMP_STACKSIZE = "192M"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM memory using openSUSE Leap 15.2

(Continued on next page)
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SPECspeed®2017_int_base = 11.8
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

General Notes (Continued)

Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDCS Sparing set to Disabled
Patrol Scrub set to Disabled
Intel Hyper-Threading Technology set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acaf64d
running on perf-blade2 Fri Nov 26 08:01:57 2021
SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo
From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6338N CPU @ 2.20GHz
  2 *physical id"s (chips)
  64 *processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 32
siblings : 32
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
  25 26 27 28 29 30 31

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SPECspeed\textsuperscript{®2017\textsubscript{int\_base}} = 11.8
SPECspeed\textsuperscript{®2017\textsubscript{int\_peak}} = 12.0

Platform Notes (Continued)

From lscpu from util-linux 2.33.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 64
On-line CPU(s) list: 0-63
Thread(s) per core: 1
Core(s) per socket: 32
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Gold 6338N CPU @ 2.20GHz
Stepping: 6
CPU MHz: 1782.480
CPU max MHz: 3500.0000
CPU min MHz: 800.0000
BogoMIPS: 4400.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 49152K
NUMA node0 CPU(s): 0-31
NUMA node1 CPU(s): 32-63
Flags: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lan constant_tsc arch_perfmon pbebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmprefp pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcpid sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invpcid_single ssbd mba ibrs ibrs Enhanced tpr_shadow vmbi fpxinor ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha ni axv512bw avx512vl xsaveopt xsavec x segment xsavec xsavec cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbb_local wbnoiw vdtherm ida arat pln pts hwp hwp_act_window hwp epp hwp_pkg_req avx512v bidi umip pku ospke avx512_vbmi2 qdfi vaes vpcmldq avx512_vnni avx512_bitalg tme avx512_vpopcntdq 1a57 rdpid md clear pconfig flush lld arch capabilities

/proc/cpuinfo cache data
cache size : 49152 KB

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CPU2017 License: 9019
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Tested by: Cisco Systems
Hardware Availability: Sep-2021
Software Availability: Sep-2021

Platform Notes (Continued)

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27
28 29 30 31
node 0 size: 1031744 MB
node 0 free: 1031175 MB
node 1 cpus: 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56
57 58 59 60 61 62 63
node 1 size: 1032180 MB
node 1 free: 1031627 MB
node distances:
node 0 1
0: 10 20
1: 20 10

From /proc/meminfo
MemTotal: 2113458748 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has
performance

From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15-SP2"
VERSION_ID="15.2"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
Linux perf-blade2 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store

(Continued on next page)
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Platform Notes (Continued)

CVE-2017-5753 (Spectre variant 1):
Bypass disabled via prctl and seccomp
Mitigation: usercopy/swapgs barriers and __user pointer sanitization

CVE-2017-5715 (Spectre variant 2):
Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

CVE-2020-0543 (Special Register Buffer Data Sampling):
Not affected

CVE-2019-11135 (TSX Asynchronous Abort):
Not affected

run-level 3 Nov 25 22:40

SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda4 btrfs 218G 41G 177G 19% /home

From /sys/devices/virtual/dmi/id
Vendor: Cisco Systems Inc
Product: UCSX-210C-M6
Serial: FCH250671KR

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200, configured at 2666

BIOS:
BIOS Vendor: Cisco Systems, Inc.
BIOS Version: X210M6.5.0.1d.0.0816211754
BIOS Date: 08/16/2021
BIOS Revision: 5.22

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C       | 600.perlbench_s(peak)
==============================================================================

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.4.0 Build 20210910_000000
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**Compiler Version Notes (Continued)**

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SPECspeed®2017_int_peak = 12.0

Cisco Systems

Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Base Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-DSPEC_OPENMP -std=c11 -m64 -fiopenmp -Wl,-z,muldefs -xCORE-AVX512
-O3 -ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/home/cpu2017/je5.0.1-64 -ljemalloc

C++ benchmarks:
-DSPEC_OPENMP -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/home/intel/compiler/2021.4.0/linux/compiler/lib/intel64_lin
-lqkmalloc

Fortran benchmarks:
-m64 -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto
-mbranches-within-32B-boundaries
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SPECspeed®2017_int_base = 11.8
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Peak Compiler Invocation

C benchmarks (except as noted below):
icx

600.perlbench_s: icc

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:

600.perlbench_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)
-xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-strict-overflow
-mbranches-within-32B-boundaries -L/home/cpu2017/je5.0.1-64
-ljemalloc

602.gcc_s: -m64 -std=c11 -Wl,-z,muldefs -fprofile-generate(pass 1)
-fprofile-use=default.profdata(pass 2) -xCORE-AVX512 -flto
-Ofast(pass 1) -O3 -ffast-math -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -L/home/cpu2017/je5.0.1-64
-ljemalloc

605.mcf_s: basepeak = yes

625.x264_s: -DSPEC_OPENMP -fiopenmp -std=c11 -m64 -Wl,-z,muldefs
-xCORE-AVX512 -flto -O3 -ffast-math
-qopt-mem-layout-trans=4 -fno-alias
-mbranches-within-32B-boundaries -L/home/cpu2017/je5.0.1-64
-ljemalloc

657.xz_s: basepeak = yes
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SPECspeed®2017_int_base = 11.8
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Peak Optimization Flags (Continued)

C++ benchmarks:
620.omnetpp_s: basepeak = yes
623.xalancbmk_s: basepeak = yes
631.deepsjeng_s: basepeak = yes
641.leela_s: basepeak = yes

Fortran benchmarks:
648.exchange2_s: basepeak = yes

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:

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