**Dell Inc.**

PowerEdge M640 (Intel Xeon Gold 5220R, 2.20 GHz)  

<table>
<thead>
<tr>
<th>Software</th>
<th><strong>SPECraté®2017_fp_base = 241</strong></th>
<th><strong>SPECraté®2017_fp_peak = 255</strong></th>
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</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Dell Inc.</td>
<td>Dell Inc.</td>
</tr>
<tr>
<td>Test Date:</td>
<td>Oct-2021</td>
<td></td>
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<tr>
<td>Hardware Availability:</td>
<td>Apr-2019</td>
<td>May-2021</td>
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</table>

### Hardware

<table>
<thead>
<tr>
<th>Copies</th>
<th>503.bwaves_r</th>
<th>507.cactuBSSN_r</th>
<th>508.namd_r</th>
<th>510.parest_r</th>
<th>511.povray_r</th>
<th>519.lbm_r</th>
<th>521.wrf_r</th>
<th>526.blender_r</th>
<th>527.cam4_r</th>
<th>538.imagick_r</th>
<th>544.nab_r</th>
<th>549.fotonik3d_r</th>
<th>554.roms_r</th>
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</tr>
</tbody>
</table>

**SPECrate®2017_fp_base** (241)  
**SPECrate®2017_fp_peak** (255)

### CPU2017 License: 55

- Test Date: Oct-2021
- Hardware Availability: Apr-2019
- Software Availability: May-2021

### CPU Name: Intel Xeon Gold 5220R

- Max MHz: 4000
- Nominal: 2200
- Enabled: 48 cores, 2 chips, 2 threads/core
- Orderable: 1.2 chips
- Cache L1: 32 KB I + 32 KB D on chip per core
- Cache L2: 1 MB I+D on chip per core
- Cache L3: 35.75 MB I+D on chip per chip
- Other: None

### Memory: 192 GB (12 x 16 GB 2Rx4 PC4-2666V-R)

- Storage: 125 GB on tmpfs
- Other: None

### OS:

Red Hat Enterprise Linux 8.4 (Ootpa)

4.18.0-305.el8.x86_64

### Compiler:

- C/C++: Version 2021.1 of Intel oneAPI DPC++/C++
- Compiler Build 20201113 for Linux;
- Fortran: Version 2021.1 of Intel Fortran Compiler
- Classic Build 20201112 for Linux;
- C/C++: Version 2021.1 of Intel C/C++ Compiler
- Classic Build 20201112 for Linux

### Parallel:

No

### Firmware:

Version 2.12.2 released Jul-2021

### File System:

tmpfs

### System State:

Run level 3 (multi-user)

### Base Pointers:

64-bit

### Peak Pointers:

64-bit

### Power Management:

BIOS and OS set to prefer performance

at the cost of additional power usage.
Dell Inc.

PowerEdge M640 (Intel Xeon Gold 5220R, 2.20 GHz)

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

Test Date: Oct-2021
Hardware Availability: Apr-2019
Software Availability: May-2021

Results Table

<table>
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<tr>
<th>Benchmark</th>
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<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/mnt/ramdisk/kavya/lib/intel64:/mnt/ramdisk/kavya/je5.0.1-64"
MALLOC_CONF = "retain:true"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM memory using Red Hat Enterprise Linux 8.1
Transparent Huge Pages enabled by default
Prior to runcpu invocation

(Continued on next page)
**Dell Inc.**

**PowerEdge M640 (Intel Xeon Gold 5220R, 2.20 GHz)**

**SPEC CPU®2017 Floating Point Rate Result**

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base</th>
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<tr>
<td>SPECrate®2017_fp_peak</td>
<td>255</td>
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</tbody>
</table>

---

**General Notes (Continued)**

Filesystem page cache synced and cleared with:
```
sync; echo 3>/proc/sys/vm/drop_caches
```
runcpu command invoked through numacl i.e.:
```
numactl --interleave=all runcpu <etc>
```
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Benchmark run from a 125 GB ramdisk created with the cmd: "mount -t tmpfs -o size=125G tmpfs /mnt/ramdisk"

---

**Platform Notes**

**BIOS Settings:**
- Sub NUMA Cluster: 2-Way Clustering
- Virtualization Technology: Disabled
- System Profile: Custom
- CPU Power Management: Maximum Performance
- C1E: Disabled
- C States: Autonomous
- Memory Patrol Scrub: Disabled
- Energy Efficiency Policy: Performance
- CPU Interconnect Bus Link
- Power Management: Disabled
- PCI ASPM L1 Link
- Power Management: Disabled

Sysinfo program /mnt/ramdisk/kavya/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acaaf64d
running on localhost.localdomain Fri Oct 29 21:17:42 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
- model name: Intel(R) Xeon(R) Gold 5220R CPU @ 2.20GHz
- 2 "physical id"s (chips)

(Continued on next page)
SPEC CPU®2017 Floating Point Rate Result

Dell Inc.

PowerEdge M640 (Intel Xeon Gold 5220R, 2.20 GHz)

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CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

Test Date: Oct-2021
Hardware Availability: Apr-2019
Software Availability: May-2021

Platform Notes (Continued)

96 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 24
siblings : 48
physical 0: cores 0 1 2 3 4 5 6 9 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29
physical 1: cores 0 1 2 3 4 5 6 9 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29

From lscpu from util-linux 2.32.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 96
On-line CPU(s) list: 0-95
Thread(s) per core: 2
Core(s) per socket: 24
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
BIOS Vendor ID: Intel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 5220R CPU @ 2.20GHz
BIOS Model name: Intel(R) Xeon(R) Gold 5220R CPU @ 2.20GHz
Stepping: 7
CPU MHz: 1940.419
CPU max MHz: 4000.0000
CPU min MHz: 1000.0000
BogoMIPS: 4400.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 36608K
NUMA node0 CPU(s):
0,4,8,12,16,20,24,28,32,36,40,44,48,52,56,60,64,68,72,76,80,84,88,92
NUMA node1 CPU(s):
1,5,9,13,17,21,25,29,33,37,41,45,49,53,57,61,65,69,73,77,81,85,89,93
NUMA node2 CPU(s):
2,6,10,14,18,22,26,30,34,38,42,46,50,54,58,62,66,70,74,78,82,86,90,94
NUMA node3 CPU(s):
Flags:
  fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
  pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
  lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
  aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
  xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave

(Continued on next page)
Dell Inc.  
PowerEdge M640 (Intel Xeon Gold 5220R, 2.20 GHz)

SPECrater®2017_fp_base = 241  
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CPU2017 License: 55  
Test Date: Oct-2021
Test Sponsor: Dell Inc.  
Hardware Availability: Apr-2019
Tested by: Dell Inc.  
Software Availability: May-2021

Platform Notes (Continued)

avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3
invpcid_single intel_ppin ssbd mba ibrs ibpb stibp ibrs_enhanced fsqsbase tsc_adjust
bmi1 hle avx2 smep bmi2 erms invpcid cqm mpx rdt_a avx512f avx512dq rdseed adx smap
ciflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaves xsaveopt xsavec xgetbv1 xsaves
cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local dtherm ida arat pln pts pku ospke
avx512_vnni md_clear flush_l1d arch_capabilities

/proc/cpuinfo cache data

(cache size : 36608 KB)

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 4 nodes (0-3)
node 0 cpus: 0 4 8 12 16 20 24 28 32 36 40 44 48 52 56 60 64 68 72 76 80 84 88 92
node 0 size: 46918 MB
node 0 free: 29167 MB
node 1 cpus: 1 5 9 13 17 21 25 29 33 37 41 45 49 53 57 61 65 69 73 77 81 85 89 93
node 1 size: 48378 MB
node 1 free: 34643 MB
node 2 cpus: 2 6 10 14 18 22 26 30 34 38 42 46 50 54 58 62 66 70 74 78 82 86 90 94
node 2 size: 48378 MB
node 2 free: 38292 MB
node 3 cpus: 3 7 11 15 19 23 27 31 35 39 43 47 51 55 59 63 67 71 75 79 83 87 91 95
node 3 size: 48341 MB
node 3 free: 39184 MB
node distances:
node 0 1 2 3
0: 10 21 11 21
1: 21 10 21 11
2: 11 21 10 21
3: 21 11 21 10

From /proc/meminfo
MemTotal: 196625832 kB
HugePages_Total: 0
Hugepagesize: 2048 kB
/sbin/tuned-adm active
  Current active profile: throughput-performance
/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
os-release:
  NAME="Red Hat Enterprise Linux"
  VERSION="8.4 (Ootpa)"

(Continued on next page)
Dell Inc.

PowerEdge M640 (Intel Xeon Gold 5220R, 2.20 GHz)

<table>
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CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

Test Date: Oct-2021
Hardware Availability: Apr-2019
Software Availability: May-2021

Platform Notes (Continued)

```bash
ID="rhel"
ID_LIKE="fedora"
VERSION_ID="8.4"
PLATFORM_ID="platform:el8"
PRETTY_NAME="Red Hat Enterprise Linux 8.4 (Ootpa)"
ANSI_COLOR="0;31"
redhat-release: Red Hat Enterprise Linux release 8.4 (Ootpa)
system-release: Red Hat Enterprise Linux release 8.4 (Ootpa)
system-release-cpe: cpe:/o:redhat:enterprise_linux:8.4:ga

uname -a:
Linux localhost.localdomain 4.18.0-305.el8.x86_64 #1 SMP Thu Apr 29 08:54:30 EDT 2021
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): KVM: Mitigation: Split huge pages
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2018-3639 (Speculative Store Bypass): Mitigation: usercopy/swapgs barriers and __user pointer sanitization
CVE-2017-5753 (Spectre variant 1): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2017-5715 (Spectre variant 2): Not affected
CVE-2020-0543 (Special Register Buffer Data Sampling): Mitigation: TSX disabled
CVE-2019-11135 (TSX Asynchronous Abort):

run-level 3 Oct 29 12:22

SPEC is set to: /mnt/ramdisk/kavya
  Filesystem  Type  Size  Used  Avail  Use%  Mounted on
  tmpfs     tmpfs  125G  44G    82G   35% /mnt/ramdisk

From /sys/devices/virtual/dmi/id
Vendor: Dell Inc.
Product: PowerEdge M640
Product Family: PowerEdge

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:

(Continued on next page)
Dell Inc.
PowerEdge M640 (Intel Xeon Gold 5220R, 2.20 GHz)

SPECrate®2017_fp_base = 241
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CPU2017 License: 55
Test Sponsor: Dell Inc.
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Test Date: Oct-2021
Hardware Availability: Apr-2019
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Platform Notes (Continued)

6x 00AD063200AD HMA82GR7AFR8N-VK 16 GB 2 rank 2666
6x 00CE063200CE M393A2K43BB1-CTD 16 GB 2 rank 2666

BIOS:
BIOS Vendor: Dell Inc.
BIOS Version: 2.12.2
BIOS Date: 07/12/2021
BIOS Revision: 2.12

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C | 519.lbm_r(base, peak) 538.imagick_r(base, peak)
   544.nab_r(base, peak)
==============================================================================

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================

C++ | 508.namd_r(base, peak) 510.parest_r(base, peak)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================

C++, C | 511.povray_r(peak)

Intel(R) C++ Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================

C++, C | 511.povray_r(base) 526.blender_r(base, peak)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113

(Continued on next page)
Dell Inc.
PowerEdge M640 (Intel Xeon Gold 5220R, 2.20 GHz)

**SPEC CPU®2017 Floating Point Rate Result**

Copyright 2017-2021 Standard Performance Evaluation Corporation

**Dell Inc.**

**PowerEdge M640 (Intel Xeon Gold 5220R, 2.20 GHz)**

**SPECraten®2017_fp_base = 241**

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**Test Date:** Oct-2021  
**Test Sponsor:** Dell Inc.  
**Hardware Availability:** Apr-2019  
**Tested by:** Dell Inc.  
**Software Availability:** May-2021

**Compiler Version Notes (Continued)**

```
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel (R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
```

```
C++, C          | 511.povray_r(peak)
```

```
Intel (R) C++ Intel (R) 64 Compiler Classic for applications running on
  Intel (R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel (R) C Intel (R) 64 Compiler Classic for applications running on Intel (R)
  64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
```

```
C++, C          | 511.povray_r(base) 526.blender_r(base, peak)
```

```
Intel (R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel (R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel (R) Fortran Intel (R) 64 Compiler Classic for applications running on
  Intel (R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
```

```
C++, C, Fortran | 507.cactuBSSN_r(base, peak)
```

```
Intel (R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel (R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel (R) Fortran Intel (R) 64 Compiler Classic for applications running on
  Intel (R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
```

```
Fortran         | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
```

```
Intel (R) Fortran Intel (R) 64 Compiler Classic for applications running on
```

(Continued on next page)
Dell Inc.
PowerEdge M640 (Intel Xeon Gold 5220R, 2.20 GHz)

SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

Dell Inc.
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Compiler Version Notes (Continued)

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==============================================================================
Fortran, C      | 521.wrf_r(peak)
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
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Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
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SPEC CPU®2017 Floating Point Rate Result
Copyright 2017-2021 Standard Performance Evaluation Corporation

Dell Inc.

PowerEdge M640 (Intel Xeon Gold 5220R, 2.20 GHz)

SPECrate®2017_fp_base = 241
SPECrate®2017_fp_peak = 255

Dell Inc.

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.
Test Date: Oct-2021
Hardware Availability: Apr-2019
Software Availability: May-2021

Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icx

Benchmarks using both C and C++:
icpx icx

Benchmarks using Fortran, C, and C++:
icpx icx ifort

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX2 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -gopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

(Continued on next page)
Dell Inc.  
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Base Optimization Flags (Continued)

C++ benchmarks:
- -w -m64 -Wl,-z,muldefs -xCORE-AVX2 -Ofast -ffast-math -flto
- -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
- -mbranches-within-32B-boundaries -ljemalloc
- -L/usr/local/jemalloc64-5.0.1/lib

Fortran benchmarks:
- -w -m64 -Wl,-z,muldefs -xCORE-AVX2 -O3 -ipo -no-prec-div
- -qopt-prefetch -ffinite-math-only
- -qopt-multiple-gather-scatter-by-shuffles -qopt-mem-layout-trans=4
- -nostandard-realloc-lhs -align array32byte -auto
- -mbranches-within-32B-boundaries -ljemalloc
- -L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using both Fortran and C:
- -w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX2 -Ofast -ffast-math
- -flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo
- -no-prec-div -qopt-prefetch -ffinite-math-only
- -qopt-multiple-gather-scatter-by-shuffles
- -mbranches-within-32B-boundaries -nostandard-realloc-lhs
- -align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using both C and C++:
- -w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX2 -Ofast -ffast-math
- -flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
- -mbranches-within-32B-boundaries -ljemalloc
- -L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using Fortran, C, and C++:
- -w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX2 -Ofast -ffast-math
- -flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3
- -no-prec-div -qopt-prefetch -ffinite-math-only
- -qopt-multiple-gather-scatter-by-shuffles
- -mbranches-within-32B-boundaries -nostandard-realloc-lhs
- -align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

Peak Compiler Invocation

C benchmarks:
- icx

C++ benchmarks:
- icpx

(Continued on next page)
Peak Compiler Invocation (Continued)

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
521.wrf_r: ifort icc
527.cam4_r: ifort icx

Benchmarks using both C and C++:
511.povray_r: icpc icc
526.blender_r: icpx icx

Benchmarks using Fortran, C, and C++:
icpx icx ifort

Peak Portability Flags
Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
519.lbm_r: basepeak = yes
538.imagick_r: basepeak = yes
544.nab_r: basepeak = yes

C++ benchmarks:
508.namd_r: basepeak = yes
510.parest_r: -w -m64 -Wl,-z,muldefs -xCORE-AVX2 -Ofast -ffast-math -flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib
Dell Inc.  
PowerEdge M640 (Intel Xeon Gold 5220R, 2.20 GHz)

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Peak Optimization Flags (Continued)

Fortran benchmarks:

503.bwaves_r:  
-w -m64 -Wl,-z,muldefs -xCORE-AVX2 -O3 -ipo  
-no-prec-div -gopt-prefetch -ffinite-math-only  
-goqpt-multiple-gather-scatter-by-shuffles  
-goqpt-mem-layout-trans=4 -nostandard-realloc-lhs  
-align array32byte -auto -mbranches-within-32B-boundaries  
-ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

549.fotonik3d_r: basepeak = yes

554.roms_r: Same as 503.bwaves_r

Benchmarks using both Fortran and C:

521.wrf_r:  
-prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2 -O3 -ipo  
-no-prec-div -goqpt-prefetch -ffinite-math-only  
-goqpt-multiple-gather-scatter-by-shuffles  
-goqpt-mem-layout-trans=4 -mbranches-within-32B-boundaries  
-nostandard-realloc-lhs -align array32byte -auto  
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

527.cam4_r: basepeak = yes

Benchmarks using both C and C++:

511.povray_r:  
-prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2 -O3 -ipo  
-no-prec-div -goqpt-prefetch -ffinite-math-only  
-goqpt-multiple-gather-scatter-by-shuffles  
-goqpt-mem-layout-trans=4 -mbranches-within-32B-boundaries  
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

526.blender_r: basepeak = yes

Benchmarks using Fortran, C, and C++:

507.cactuBSSN_r: basepeak = yes

---

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml  
http://www.spec.org/cpu2017/flags/Dell-Platform-Flags-PowerEdge-Intel-ICX-rev1.4.xml
## SPEC CPU®2017 Floating Point Rate Result

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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