Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6312U, 2.40GHz)

SPECrates®2017_fp_base = 182
SPECrates®2017_fp_peak = 184

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<th>CPU2017 License:</th>
<th>9019</th>
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<td>Test Sponsor:</td>
<td>Cisco Systems</td>
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<td>Tested by:</td>
<td>Cisco Systems</td>
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<td>Test Date:</td>
<td>Sep-2021</td>
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<tr>
<td>Hardware Availability:</td>
<td>Apr-2021</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>Dec-2020</td>
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<table>
<thead>
<tr>
<th>Software</th>
<th>Hardware</th>
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<tbody>
<tr>
<td>OS: SUSE Linux Enterprise Server 15 SP2 (x86_64) 5.3.18-22-default</td>
<td>CPU Name: Intel Xeon Gold 6312U</td>
</tr>
<tr>
<td>Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux; Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux; C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux</td>
<td>Max MHz: 3600</td>
</tr>
<tr>
<td>Firmware: Version 4.2.1d released Jul-2021</td>
<td>Nominal: 2400</td>
</tr>
<tr>
<td>File System: btrfs</td>
<td>Enabled: 24 cores, 1 chip, 2 threads/core</td>
</tr>
<tr>
<td>System State: Run level 3 (multi-user)</td>
<td>Orderable: 1 Chips</td>
</tr>
<tr>
<td>Base Pointers: 64-bit</td>
<td>Cache L1: 32 KB I + 48 KB D on chip per core</td>
</tr>
<tr>
<td>Peak Pointers: 64-bit</td>
<td>L2: 1.25 MB I+D on chip per core</td>
</tr>
<tr>
<td>Other: jemalloc memory allocator V5.0.1</td>
<td>L3: 36 MB I+D on chip per chip</td>
</tr>
<tr>
<td>Power Management: BIOS and OS set to prefer performance at the cost of additional power usage</td>
<td>Other: None</td>
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## Results Table

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</tbody>
</table>

**Submit Notes**

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

**Operating System Notes**

Stack size set to unlimited using "ulimit -s unlimited"

**Environment Variables Notes**

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOCONF = "retain:true"

**General Notes**

Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
```
sync; echo 3> /proc/sys/vm/drop_caches
```

(Continued on next page)
General Notes (Continued)

runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Settings:
    Adjacent Cache Line Prefetcher set to Disabled
    DCU Streamer Prefetch set to Disabled
    UPI Link Enablement set to 1
    UPI Power Management set to Enabled
    Sub NUMA Clustering set to Enabled
    LLC Dead Line set to Disabled
    Memory Refresh Rate set to 1x Refresh
    ADDDC Sparing set to Disabled
    Patrol Scrub set to Disabled
    Energy Efficient Turbo set to Enabled
    Processor C6 Report set to Enabled
    Processor C1E set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16a6acaf64d
running on localhost Tue Sep 28 19:12:53 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
    https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
    model name : Intel(R) Xeon(R) Gold 6312U CPU @ 2.40GHz
    1 "physical id"s (chips)
    48 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 24
siblings : 48
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23

(Continued on next page)
## SPEC CPU®2017 Floating Point Rate Result

**Cisco Systems**  
Cisco UCS C220 M6 (Intel Xeon Gold 6312U, 2.40GHz)

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**CPU2017 License:** 9019  
**Test Date:** Sep-2021  
**Test Sponsor:** Cisco Systems  
**Hardware Availability:** Apr-2021  
**Tested by:** Cisco Systems  
**Software Availability:** Dec-2020

### Platform Notes (Continued)

From `lscpu` from `util-linux 2.33.1`:

- **Architecture:** x86_64
- **CPU op-mode(s):** 32-bit, 64-bit
- **Byte Order:** Little Endian
- **Address sizes:** 46 bits physical, 57 bits virtual
- **CPU(s):** 48
- **On-line CPU(s) list:** 0-47
- **Thread(s) per core:** 2
- **Core(s) per socket:** 24
- **Vendor ID:** GenuineIntel
- **CPU family:** 6
- **Model:** 106
- **Model name:** Intel(R) Xeon(R) Gold 6312U CPU @ 2.40GHz
- **Stepping:** 6
- **CPU MHz:** 3128.495
- **CPU max MHz:** 3600.0000
- **CPU min MHz:** 800.0000
- **BogoMIPS:** 4800.00
- **Virtualization:** VT-x
- **L1d cache:** 48K
- **L1i cache:** 32K
- **L2 cache:** 1280K
- **L3 cache:** 36864K
- **NUMA node0 CPU(s):** 0-11, 24-35
- **NUMA node1 CPU(s):** 12-23, 36-47

**Flags:** fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pciid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 invpcid_single ssbd mba ibpb ibrs Enhanced tpr_shadow vmla flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha ni avx512bw avx512vl xsaves xsaveopt xsavevc xsavec qsmm_llc qsmm_occupy_llc qsmm_mbb_total qsmm_mbb_local wbinvd dtherm ida arat pln pts hwlp wwp-act_window wwp-ep wwp-pkg-req avx512vbmi umip kpu ospe avx512_vbmi2 gfnl vaes vpcmldqsd avx512_vnni avx512_bitalg tme avx512_vpopcntdq 1a57 rdpid md_clear pconfig flush_lid arch_capabilities

/proc/cpuinfo cache data  
**cache size:** 36864 KB

From `numactl --hardware`  
**WARNING:** a numactl 'node' might or might not correspond to a physical chip.

(Continued on next page)
Platform Notes (Continued)

available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 24 25 26 27 28 29 30 31 32 33 34 35
node 0 size: 257529 MB
node 0 free: 243133 MB
node 1 cpus: 12 13 14 15 16 17 18 19 20 21 22 23 36 37 38 39 40 41 42 43 44 45 46 47
node 1 size: 257764 MB
node 1 free: 246578 MB
node distances:
node 0 1
  0:  10  11
  1:  11  10

From /proc/meminfo
MemTotal:       527661304 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
NAME="SLES"
VERSION="15-SP2"
VERSION_ID="15.2"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
Linux localhost 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs barriers and __user pointer sanitization

(Continued on next page)
Cisco Systems
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Test Date: Sep-2021
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Platform Notes (Continued)

CVE-2017-5715 (Spectre variant 2):
Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling):
Not affected
CVE-2019-11135 (TSX Asynchronous Abort):
Not affected

run-level 3 Sep 28 12:16
SPEC is set to: /home/cpu2017

Filesystem     Type   Size  Used Avail Use% Mounted on
/dev/sda2      btrfs  222G   53G  169G  24% /home

From /sys/devices/virtual/dmi/id
Vendor:         Cisco Systems Inc
Product:        UCSC-C220-M6S
Serial:         WZP24430N7F

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
  16x 0xCE00 M393A4K40DB3-CWE 32 GB 2 rank 3200
  16x NO DIMM NO DIMM

BIOS:
  BIOS Vendor:    Cisco Systems, Inc.
  BIOS Version:   C220M6.4.2.id.0.0730210924
  BIOS Date:      07/30/2021
  BIOS Revision:  5.22

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C               | 519.lbm_r(base, peak) 538.imagick_r(base, peak)
| 544.nab_r(base, peak)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================

C++             | 508.namd_r(base, peak) 510.parest_r(base, peak)

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==============================================================================
C++, C          | 511.povray_r(peak)
Intel(R) C++ Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
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==============================================================================
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
   Intel(R) 64, Version 2021.1 Build 20201112_000000
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==============================================================================
Fortran, C      | 521.wrf_r(base) 527.cam4_r(base, peak)
==============================================================================
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
   Intel(R) 64, Version 2021.1 Build 20201112_000000
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Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
   Version 2021.1 Build 20201113
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==============================================================================

Base Compiler Invocation
C benchmarks:
icx
C++ benchmarks:
icpx
Fortran benchmarks:
ifort
Benchmarks using both Fortran and C:
ifort icx
Benchmarks using both C and C++:
icpx icx
Benchmarks using Fortran, C, and C++:
icpx icx ifort
### SPEC CPU®2017 Floating Point Rate Result

**Cisco Systems**
Cisco UCS C220 M6 (Intel Xeon Gold 6312U, 2.40GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base</th>
<th>SPECrate®2017_fp_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>182</td>
<td>184</td>
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</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Sep-2021  
**Hardware Availability:** Apr-2021  
**Software Availability:** Dec-2020

#### Base Portability Flags

- 503.bwaves_r: -DSPEC_LP64
- 507.cactuBSSN_r: -DSPEC_LP64
- 508.namd_r: -DSPEC_LP64
- 510.prest_r: -DSPEC_LP64
- 511.povray_r: -DSPEC_LP64
- 519.1bm_r: -DSPEC_LP64
- 521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
- 526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
- 527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
- 538.imagick_r: -DSPEC_LP64
- 544.nab_r: -DSPEC_LP64
- 549.fotonik3d_r: -DSPEC_LP64
- 554.roms_r: -DSPEC_LP64

#### Base Optimization Flags

**C benchmarks:**
- -w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
- -flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
- -mbranches-within-32B-boundaries -ljemalloc
- -L/usr/local/jemalloc64-5.0.1/lib

**C++ benchmarks:**
- -w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -flto
- -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
- -mbranches-within-32B-boundaries -ljemalloc
- -L/usr/local/jemalloc64-5.0.1/lib

**Fortran benchmarks:**
- -w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
- -qopt-prefetch -ffinite-math-only
- -qopt-multiple-gather-scatter-by-shuffles -qopt-mem-layout-trans=4
- -nostandard-realloc-lhs -align array32byte -auto
- -mbranches-within-32B-boundaries -ljemalloc
- -L/usr/local/jemalloc64-5.0.1/lib

**Benchmarks using both Fortran and C:**
- -w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
- -flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo
- -no-prec-div -qopt-prefetch -ffinite-math-only
- -qopt-multiple-gather-scatter-by-shuffles
- -mbranches-within-32B-boundaries -nostandard-realloc-lhs
- -align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

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Base Optimization Flags (Continued)

Benchmarks using both C and C++:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-fflto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using Fortran, C, and C++:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-fflto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

Peak Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:	ifort

Benchmarks using both Fortran and C:
521.wrf_r: ifort icc
527.cam4_r: ifort icx

Benchmarks using both C and C++:
511.povray_r: icpc icc
526.blender_r: icpx icx

Benchmarks using Fortran, C, and C++:
icpx icx ifort
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Cisco UCS C220 M6 (Intel Xeon Gold 6312U, 2.40GHz)

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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Sep-2021
Tested by: Cisco Systems
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Peak Portability Flags
Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
519.lbm_r: basepeak = yes
538.imagick_r: basepeak = yes
544.nab_r: -w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -flto -Ofast -qopt-mem-layout-trans=4 -flto -mbranches-within-32B-boundaries -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

C++ benchmarks:
508.namd_r: basepeak = yes

Fortran benchmarks:
549.fotonik3d_r: basepeak = yes
554.roms_r: Same as 503.bwaves_r

Benchmarks using both Fortran and C:
521.wrf_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-multiple-gather-scatter-by-shuffles -qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries

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Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6312U, 2.40GHz)

**SPECrate®2017_fp_base = 182**
**SPECrate®2017_fp_peak = 184**

Peak Optimization Flags (Continued)

521.wrf_r (continued):
- nostandard-realloc-lhs -align array32byte -auto
- L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

527.cam4_r: basepeak = yes

Benchmarks using both C and C++:

511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3
-ipo -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

526.blender_r: basepeak = yes

Benchmarks using Fortran, C, and C++:

507.cactuBSSN_r: basepeak = yes

The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:

http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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