# SPEC CPU®2017 Integer Rate Result

## Cisco Systems

Cisco UCS C225 M6 (AMD EPYC 7643 48-Core Processor)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>679</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_int_peak</td>
<td>712</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Sep-2021  
**Hardware Availability:** Jun-2021  
**Software Availability:** Jun-2021

### Hardware

<table>
<thead>
<tr>
<th>Copies</th>
<th>SPECrate®2017_int_base (679)</th>
<th>SPECrate®2017_int_peak (712)</th>
</tr>
</thead>
<tbody>
<tr>
<td>500perlbench_r 192</td>
<td>465</td>
<td>598</td>
</tr>
<tr>
<td>502gcc_r 192</td>
<td>532</td>
<td></td>
</tr>
<tr>
<td>505mcf_r 192</td>
<td>662</td>
<td></td>
</tr>
<tr>
<td>520omnetpp_r 192</td>
<td>875</td>
<td></td>
</tr>
<tr>
<td>523xalanchmk_r 192</td>
<td>941</td>
<td></td>
</tr>
<tr>
<td>525x264_r 192</td>
<td>773</td>
<td></td>
</tr>
<tr>
<td>531deepsjeng_r 192</td>
<td>840</td>
<td></td>
</tr>
<tr>
<td>541leela_r 192</td>
<td>1420</td>
<td></td>
</tr>
<tr>
<td>548.exchange2_r 192</td>
<td>1510</td>
<td></td>
</tr>
<tr>
<td>557xz_r 192</td>
<td>409</td>
<td></td>
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<tr>
<td>410</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**CPU Name:** AMD EPYC 7643  
**Max MHz:** 3600  
**Nominal:** 2300  
**Enabled:** 96 cores, 2 chips, 2 threads/core  
**Orderable:** 1.2 chips  
**Cache L1:** 32 KB I + 32 KB D on chip per core  
**L2:** 512 KB I+D on chip per core  
**L3:** 256 MB I+D on chip per chip, 32 MB shared / 6 cores  
**Other:** None  
**Memory:** 2 TB (16 x 128 GB 4Rx4 PC4-3200V-L)  
**Storage:** 1 x 960 GB M.2 SSD SATA  
**Other:** None

### Software

**OS:** SUSE Linux Enterprise Server 15 SP3 (x86_64) kernel version 5.3.18-57-default  
**Compiler:** C/C++/Fortran: Version 3.0.0 of AOCC  
**Parallel:** No  
**Firmware:** Version C225M6.4.2.1c released Sep-2021  
**File System:** xfs  
**System State:** Run level 3 (multi-user)  
**Base Pointers:** 64-bit  
**Peak Pointers:** 32/64-bit  
**Other:** jemalloc: jemalloc memory allocator library v5.1.0  
**Power Management:** BIOS and OS set to prefer performance at the cost of additional power usage
## Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlibench_r</td>
<td>192</td>
<td>662</td>
<td>462</td>
<td>657</td>
<td>465</td>
<td>656</td>
<td>466</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>192</td>
<td>511</td>
<td>532</td>
<td>513</td>
<td>530</td>
<td>508</td>
<td>535</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>192</td>
<td>355</td>
<td>875</td>
<td>354</td>
<td>877</td>
<td>355</td>
<td>873</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>192</td>
<td>764</td>
<td>330</td>
<td>761</td>
<td>331</td>
<td>765</td>
<td>329</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>192</td>
<td>262</td>
<td>773</td>
<td>264</td>
<td>767</td>
<td>261</td>
<td>776</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>192</td>
<td>239</td>
<td>1410</td>
<td>236</td>
<td>1420</td>
<td>237</td>
<td>1420</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>192</td>
<td>350</td>
<td>630</td>
<td>350</td>
<td>629</td>
<td>351</td>
<td>627</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>192</td>
<td>468</td>
<td>680</td>
<td>470</td>
<td>677</td>
<td>469</td>
<td>678</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>192</td>
<td>333</td>
<td>1510</td>
<td>332</td>
<td>1510</td>
<td>320</td>
<td>1570</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>192</td>
<td>507</td>
<td>409</td>
<td>506</td>
<td>410</td>
<td>507</td>
<td>409</td>
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### Compiler Notes

The AMD64 AOCC Compiler Suite is available at http://developer.amd.com/amd-aocc/

### Submit Notes

The config file option 'submit' was used. 'numactl' was used to bind copies to the cores. See the configuration file for details.

### Operating System Notes

'ulimit -s unlimited' was used to set environment stack size limit
'ulimit -l 2097152' was used to set environment locked pages in memory limit runcpu command invoked through numacl1 i.e.:
numactl --interleave=all runcpu <etc>
'echo 8 > /proc/sys/vm/dirty_ratio' run as root to limit dirty cache to 8% of memory.
'echo 1 > /proc/sys/vm/swappiness' run as root to limit swap usage to minimum necessary.
'echo 1 > /proc/sys/vm/zone_reclaim_mode' run as root to free node-local memory and avoid remote memory usage.
'sync; echo 3 > /proc/sys/vm/drop_caches' run as root to reset filesystem caches.
'sysctl -w kernel.randomize_va_space=0' run as root to disable address space layout randomization (ASLR) to reduce run-to-run variability.

(Continued on next page)
Cisco Systems
Cisco UCS C225 M6 (AMD EPYC 7643 48-Core Processor)

SPEC CPU®2017 Integer Rate Result
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SPECrate®2017_int_base = 679
SPECrate®2017_int_peak = 712

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Sep-2021
Hardware Availability: Jun-2021
Software Availability: Jun-2021

Operating System Notes (Continued)
'echo always > /sys/kernel/mm/transparent_hugepage/enabled' and
'echo always > /sys/kernel/mm/transparent_hugepage/defrag' run as root for peak
integer runs and all FP runs to enable Transparent Hugepages (THP).

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH =
"/home/cpu2017/amd_rate_aocc300_milan_B_lib/lib;/home/cpu2017/amd_rate_a
cocc300_milan_B_lib/lib32;"
MALLOCONF = "retain:true"

Environment variables set by runcpu during the 523.xalancbmk_r peak run:
MALLOCONF = "thp:never"

General Notes
Binaries were compiled on a system with 2x AMD EPYC 7742 CPU + 1TiB Memory using OpenSUSE 15.2

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
jemalloc: configured and built with GCC v4.8.2 in RHEL 7.4 (No options specified)
jemalloc 5.1.0 is available here:
https://github.com/jemalloc/jemalloc/releases/download/5.1.0/jemalloc-5.1.0.tar.bz2

Platform Notes
BIOS Configuration
SMT Mode set to Auto
NUMA nodes per socket set to NPS4
ACPI SRAT L3 Cache As NUMA Domain set to Enabled
DRAM Scrub Time set to Disabled
Determinism Slider set to Power
Memory Interleaving set to Auto
APBDIS set to 1

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16aaca64d

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Platform Notes (Continued)

running on localhost Fri Sep 17 03:24:38 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name: AMD EPYC 7643 48-Core Processor
  2 "physical id"s (chips)
  192 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores: 48
siblings: 96
physical 0: cores 0 1 2 3 4 5 8 9 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29
32 33 34 35 36 37 40 41 42 43 44 45 48 49 50 51 52 53 56 57 58 59 60 61
physical 1: cores 0 1 2 3 4 5 8 9 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29
32 33 34 35 36 37 40 41 42 43 44 45 48 49 50 51 52 53 56 57 58 59 60 61

From lscpu from util-linux 2.36.2:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 48 bits physical, 48 bits virtual
CPU(s): 192
On-line CPU(s) list: 0-191
Thread(s) per core: 2
Core(s) per socket: 48
Socket(s): 2
NUMA node(s): 16
Vendor ID: AuthenticAMD
CPU family: 25
Model: 1
Model name: AMD EPYC 7643 48-Core Processor
Stepping: 1
Frequency boost: enabled
CPU MHz: 1543.659
CPU max MHz: 2300.0000
CPU min MHz: 1500.0000
BogoMIPS: 4591.15
Virtualization: AMD-V
L1d cache: 3 MiB
L1i cache: 3 MiB
L2 cache: 48 MiB
L3 cache: 512 MiB
NUMA node0 CPU(s): 0-5,96-101
NUMA node1 CPU(s): 6-11,102-107

(Continued on next page)
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Platform Notes (Continued)

NUMA node2 CPU(s): 12-17, 108-113
NUMA node3 CPU(s): 18-23, 114-119
NUMA node4 CPU(s): 24-29, 120-125
NUMA node5 CPU(s): 30-35, 126-131
NUMA node6 CPU(s): 36-41, 132-137
NUMA node7 CPU(s): 42-47, 138-143
NUMA node8 CPU(s): 48-53, 144-149
NUMA node9 CPU(s): 54-59, 150-155
NUMA node10 CPU(s): 60-65, 156-161
NUMA node11 CPU(s): 66-71, 162-167
NUMA node12 CPU(s): 72-77, 168-173
NUMA node13 CPU(s): 78-83, 174-179
NUMA node14 CPU(s): 84-89, 180-185
NUMA node15 CPU(s): 90-95, 186-191

Vulnerability Itlb multihit: Not affected
Vulnerability L1tf: Not affected
Vulnerability Mds: Not affected
Vulnerability Meltdown: Not affected
Vulnerability Spec store bypass: Mitigation; Speculative Store Bypass disabled via prctl and seccomp
Vulnerability Spectre v1: Mitigation; usercopy/swapgs barriers and __user pointer sanitization
Vulnerability Spectre v2: Mitigation; Full AMD retpoline, IBPB conditional, IBRS_FW, STIBBP always-on, RSB filling
Vulnerability Srbd: Not affected
Vulnerability Tsx async abort: Not affected

Flags:

From lscpu --cache:

NAME ONE-SIZE ALL-SIZE WAYS TYPE LEVEL SETS PHY-LINE COHERENCY-SIZE
L1d 32K 3M 8 Data 1 64 1 64
L1i 32K 3M 8 Instruction 1 64 1 64
L2 512K 48M 8 Unified 2 1024 1 64
L3 32M 512M 16 Unified 3 32768 1 64

(Continued on next page)
## Platform Notes (Continued)

/platform/cpuminfo cache data
  cache size : 512 KB

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
  available: 16 nodes (0-15)
  node 0 cpus: 0 1 2 3 4 5 96 97 98 99 100 101
  node 0 size: 128802 MB
  node 0 free: 128212 MB
  node 1 cpus: 6 7 8 9 10 11 102 103 104 105 106 107
  node 1 size: 129018 MB
  node 1 free: 128792 MB
  node 2 cpus: 12 13 14 15 16 17 108 109 110 111 112 113
  node 2 size: 129020 MB
  node 2 free: 128792 MB
  node 3 cpus: 18 19 20 21 22 23 114 115 116 117 118 119
  node 3 size: 129018 MB
  node 3 free: 128845 MB
  node 4 cpus: 24 25 26 27 28 29 120 121 122 123 124 125
  node 4 size: 129020 MB
  node 4 free: 128633 MB
  node 5 cpus: 30 31 32 33 34 35 126 127 128 129 130 131
  node 5 size: 129018 MB
  node 5 free: 128819 MB
  node 6 cpus: 36 37 38 39 40 41 132 133 134 135 136 137
  node 6 size: 129020 MB
  node 6 free: 128841 MB
  node 7 cpus: 42 43 44 45 46 47 138 139 140 141 142 143
  node 7 size: 129006 MB
  node 7 free: 128827 MB
  node 8 cpus: 48 49 50 51 52 53 144 145 146 147 148 149
  node 8 size: 129020 MB
  node 8 free: 128838 MB
  node 9 cpus: 54 55 56 57 58 59 150 151 152 153 154 155
  node 9 size: 129018 MB
  node 9 free: 128851 MB
  node 10 cpus: 60 61 62 63 64 65 156 157 158 159 160 161
  node 10 size: 129020 MB
  node 10 free: 128829 MB
  node 11 cpus: 66 67 68 69 70 71 162 163 164 165 166 167
  node 11 size: 129018 MB
  node 11 free: 128840 MB
  node 12 cpus: 72 73 74 75 76 77 168 169 170 171 172 173
  node 12 size: 129020 MB
  node 12 free: 128838 MB
  node 13 cpus: 78 79 80 81 82 83 174 175 176 177 178 179
  node 13 size: 129018 MB

(Continued on next page)
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**SPECrate®2017_int_base = 679**

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**Platform Notes (Continued)**

node 13 free: 128832 MB
node 14 cpus: 84 85 86 87 88 89 180 181 182 183 184 185
node 14 size: 129020 MB
node 14 free: 128750 MB
node 15 cpus: 90 91 92 93 94 95 186 187 188 189 190 191
node 15 size: 129018 MB
node 15 free: 128815 MB

node distances:

<table>
<thead>
<tr>
<th>node</th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
<th>11</th>
<th>12</th>
<th>13</th>
<th>14</th>
<th>15</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>10</td>
<td>11</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
</tr>
<tr>
<td>1</td>
<td>11</td>
<td>10</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
</tr>
<tr>
<td>2</td>
<td>12</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>12</td>
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<td>12</td>
<td>12</td>
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<td>32</td>
</tr>
<tr>
<td>3</td>
<td>12</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
</tr>
<tr>
<td>4</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>10</td>
<td>11</td>
<td>12</td>
<td>12</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
</tr>
<tr>
<td>5</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>12</td>
<td>12</td>
<td>32</td>
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<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
</tr>
<tr>
<td>6</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>10</td>
<td>11</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
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<tr>
<td>7</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>32</td>
<td>32</td>
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<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
</tr>
<tr>
<td>8</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>10</td>
<td>11</td>
<td>12</td>
<td>12</td>
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<td>12</td>
<td>12</td>
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<tr>
<td>9</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>32</td>
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<td>12</td>
<td>12</td>
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<td>32</td>
<td>32</td>
<td>32</td>
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<td>32</td>
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<td>32</td>
<td>32</td>
<td>12</td>
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<td>12</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>12</td>
</tr>
</tbody>
</table>

From `/proc/meminfo`

- MemTotal: 2113625640 kB
- HugePages_Total: 0
- Hugepagesize: 2048 kB

`/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor` has `ondemand`

From `/etc/*release* /etc/*version*`

- os-release:
  - NAME="SLES"
  - VERSION="15-SP3"
  - VERSION_ID="15.3"
  - PRETTY_NAME="SUSE Linux Enterprise Server 15 SP3"
  - ID="sles"
  - ID_LIKE="suse"
  - ANSI_COLOR="0;32"
  - CPE_NAME="cpe:/o:suse:sles:15:sp3"

`uname -a`:

Linux localhost 5.3.18-57-default #1 SMP Wed Apr 28 10:54:41 UTC 2021 (ba3c2e9) x86_64

(Continued on next page)
Cisco Systems
Cisco UCS C225 M6 (AMD EPYC 7643 48-Core Processor)

SPEC CPU®2017 Integer Rate Result
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Cisco Systems
Cisco UCS C225 M6 (AMD EPYC 7643 48-Core Processor)

SPECrate®2017_int_base = 679
SPECrate®2017_int_peak = 712

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Sep-2021
Hardware Availability: Jun-2021
Software Availability: Jun-2021

Platform Notes (Continued)

x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp

CVE-2017-5753 (Spectre variant 1): Mitigation: userscopy/swapgs barriers and __user pointer sanitation
CVE-2017-5715 (Spectre variant 2): Mitigation: Full AMD retpoline, IBPB: conditional, IBRS_FW, STIBP: always-on, RSB filling

CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Sep 17 03:24

SPEC is set to: /home/cpu2017
Filesystem    Type  Size  Used Avail Use% Mounted on
/dev/sdb3      xfs   557G   11G  546G   2% /

From /sys/devices/virtual/dmi/id
Vendor: Cisco Systems Inc
Product: UCSC-C225-M6S
Serial: WZP252309U3

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
16x 0xCE00 M386AAG40AM3-CWE 128 GB 4 rank 3200

BIOS:
BIOS Vendor: Cisco Systems, Inc.
BIOS Version: C225M6.4.2.1c.0.0806211349
BIOS Date: 08/06/2021
BIOS Revision: 5.22

(End of data from sysinfo program)
Cisco Systems
Cisco UCS C225 M6 (AMD EPYC 7643 48-Core Processor)

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**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Test Date:** Sep-2021  
**Tested by:** Cisco Systems  
**Hardware Availability:** Jun-2021  
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### Compiler Version Notes

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<td>C</td>
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<td></td>
<td>502.gcc_r(peak)</td>
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<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>AMD clang version 12.0.0 (CLANG: AOCC_3.0.0-Build#78 2020_12_10) (based on LLVM Mirror.Version.12.0.0)</td>
<td></td>
<td></td>
<td>i386-unknown-linux-gnu</td>
<td>posix</td>
<td>/opt/AMD/aocc-compiler-3.0.0/bin</td>
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<td>523.xalancbmk_r(peak)</td>
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Cisco Systems
Cisco UCS C225 M6 (AMD EPYC 7643 48-Core Processor)

| SPECrate®2017_int_base = 679 | SPECrate®2017_int_peak = 712 |

CPU2017 License: 9019  |  Test Date:  | Sep-2021 |
Test Sponsor: Cisco Systems  |  Hardware Availability:  | Jun-2021 |
Tested by: Cisco Systems  |  Software Availability:  | Jun-2021 |

Compiler Version Notes (Continued)

Target: i386-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.0.0/bin

---

| C++ | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base) |
|     | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak) |

AMD clang version 12.0.0 (CLANG: AOCC_3.0.0-Build#78 2020_12_10) (based on LLVM Mirror.Version.12.0.0)
Target: x86_64-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.0.0/bin

---

| C++ | 523.xalancbmk_r(peak) |

---

| C++ | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base) |
|     | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak) |

AMD clang version 12.0.0 (CLANG: AOCC_3.0.0-Build#78 2020_12_10) (based on LLVM Mirror.Version.12.0.0)
Target: x86_64-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.0.0/bin

---

| Fortran | 548.exchange2_r(base, peak) |

---

| Fortran | 548.exchange2_r(base, peak) |

AMD clang version 12.0.0 (CLANG: AOCC_3.0.0-Build#78 2020_12_10) (based on LLVM Mirror.Version.12.0.0)
Target: x86_64-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.0.0/bin
SPEC CPU®2017 Integer Rate Result

Cisco Systems
Cisco UCS C225 M6 (AMD EPYC 7643 48-Core Processor)

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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Sep-2021
Hardware Availability: Jun-2021
Software Availability: Jun-2021

Base Compiler Invocation

C benchmarks:
clang

C++ benchmarks:
clang++

Fortran benchmarks:
flang

Base Portability Flags

500.perlbench_r: -DSPEC_LINUX_X64 -DSPEC_LP64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LINUX -DSPEC_LP64
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
m64 -Wl,-allow-multiple-definition -Wl,-mllvm -Wl,-disable-licm-vrp
-mfllto -Wl,-mllvm -Wl,-region-vectorize
-Wl,-mllvm -Wl,-function-specialize
-Wl,-mllvm -Wl,-align-all-nofallthru-blocks=6
-Wl,-mllvm -Wl,-reduce-array-computations=3 -03 -ffast-math
-march=znver3 -fveclib=AMDLIBM -fstruct-layout=5
-mllvm -unroll-threshold=50 -mllvm -inline-threshold=1000
-freemap-arrays -mllvm -function-specialize -flv-function-specialization
-mllvm -enable-gvn-hoist -mllvm -global-vectorize-slp=true
-mllvm -enable-licm-vrp -mllvm -reduce-array-computations=3 -z muldefs
-lamdlibm -ljemalloc -lflang -lflangrti

C++ benchmarks:
m64 -std=c++98 -Wl,-mllvm -Wl,-do-block-reorder-aggressive -flto
-Wl,-mllvm -Wl,-region-vectorize -Wl,-mllvm -Wl,-function-specialize
-Wl,-mllvm -Wl,-align-all-nofallthru-blocks=6
-Wl,-mllvm -Wl,-reduce-array-computations=3 -03 -ffast-math

(Continued on next page)
Cisco Systems
Cisco UCS C225 M6 (AMD EPYC 7643 48-Core Processor)

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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Sep-2021
Hardware Availability: Jun-2021
Tested by: Cisco Systems
Software Availability: Jun-2021

### Base Optimization Flags (Continued)

C++ benchmarks (continued):
- -march=znver3 -fveclib=AMDLIBM -mllvm -enable-partial-unswitch
- -mllvm -unroll-threshold=100 -finline-aggressive
- -flv-function-specialization -mllvm -loop-unswitch-threshold=200000
- -mllvm -reroll-loops -mllvm -aggressive-loop-unswitch
- -mllvm -extra-vectorizer-passes -mllvm -reduce-array-computations=3
- -mllvm -global-vectorize-slp=true -mllvm -convert-pow-exp-to-int=false
- -z muldefs -mllvm -do-block-reorder=aggressive
- -fvirtual-function-elimination -fvisibility=hidden -lamdlibm
- -ljemalloc -lflang -lflangrti

Fortran benchmarks:
- -m64 -Wl, -mllvm -Wl, -inline-recursion=4
- -Wl, -mllvm -Wl, -isr-in-nested-loop -Wl, -mllvm -Wl, -enable-iv-split
- -flto -Wl, -mllvm -Wl, -region-vectorize
- -Wl, -mllvm -Wl, -function-specialize
- -Wl, -mllvm -Wl, -align-all-nofallthru-blocks=6
- -Wl, -mllvm -Wl, -reduce-array-computations=3 -O3 -ffast-math
- -march=znver3 -fveclib=AMDLIBM -z muldefs -mllvm -unroll-aggressive
- -mllvm -unroll-threshold=500 -lamdlibm -ljemalloc -lflang -lflangrti

### Base Other Flags

C benchmarks:
- -Wno-unused-command-line-argument

C++ benchmarks:
- -Wno-unused-command-line-argument

### Peak Compiler Invocation

C benchmarks:
clang

C++ benchmarks:
clang++

Fortran benchmarks:
flang
Cisco Systems
Cisco UCS C225 M6 (AMD EPYC 7643 48-Core Processor)

SPEC®2017_int_base = 679
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Sep-2021
Hardware Availability: Jun-2021
Software Availability: Jun-2021

Peak Portability Flags

500.perlbench_r: -DSPEC_LINUX_X64 -DSPEC_LP64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LINUX -DSPEC_LP64
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

(Continued on next page)

Peak Optimization Flags

C benchmarks:

500.perlbench_r: -m64 -Wl,-allow-multiple-definition
-Wl,-mlllvm -Wl,-enable-liecm-vrp -flito
-Wl,-mlllvm -Wl,-function-specialize
-Wl,-mlllvm -Wl,-align-all-nofallthru-blocks=6
-Wl,-mlllvm -Wl,-reduce-array-computations=3
-ffprofile-instr-generate(pass 1)
-ffprofile-instr-use(pass 2) -Ofast -march=zmmver3
-fveclib=AMDLIBM -fstruct-layout=7
-mlllvm -unroll-threshold=50 -fremap-arrays
-flv-function-specialization -mlllvm -inline-threshold=1000
-mlllvm -enable-gvn-hoist -mlllvm -global-vectorize-slp=false
-mlllvm -function-specialize -mlllvm -enable-liecm-vrp
-mlllvm -reduce-array-computations=3 -lammllibm -ljemalloc

502.gcc_r: -m32 -Wl,-allow-multiple-definition
-Wl,-mlllvm -Wl,-enable-liecm-vrp -flito
-Wl,-mlllvm -Wl,-function-specialize -Ofast -march=zmmver3
-fveclib=AMDLIBM -fstruct-layout=7
-mlllvm -unroll-threshold=50 -fremap-arrays
-flv-function-specialization -mlllvm -inline-threshold=1000
-mlllvm -enable-gvn-hoist -mlllvm -global-vectorize-slp=true
-mlllvm -function-specialize -mlllvm -enable-liecm-vrp
-mlllvm -reduce-array-computations=3 -fgnu89-inline
-ljemalloc

505.mcf_r: -m64 -Wl,-allow-multiple-definition
-Wl,-mlllvm -Wl,-enable-liecm-vrp -flito
-Wl,-mlllvm -Wl,-function-specialize
-Wl,-mlllvm -Wl,-align-all-nofallthru-blocks=6

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

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Peak Optimization Flags (Continued)

505.mcf_r (continued):
-W1,-mllvm -W1,-reduce-array-computations=3 -Ofast
-march=znver3 -fveclib=AMDLIBM -fstruct-layout=7
-mllvm -unroll-threshold=50 -fremap-arrays
-flv-function-specialization -mllvm -inline-threshold=1000
-mllvm -enable-gvn-hoist -mllvm -global-vectorize-slp=true
-mllvm -function-specialize -mllvm -enable-licm-vrp
-mllvm -reduce-array-computations=3 -lamdlibm -ljemalloc

525.x264_r: basepeak = yes

557.xz_r: Same as 505.mcf_r

C++ benchmarks:

520.omnetpp_r: -m64 -std=c++98
-W1,-mllvm -W1,-do-block-reorder=aggressive -flto
-W1,-mllvm -W1,-function-specialize
-W1,-mllvm -W1,-align-all-nofallthru-blocks=6
-W1,-mllvm -W1,-reduce-array-computations=3 -Ofast
-march=znver3 -fveclib=AMDLIBM -finline-aggressive
-mllvm -unroll-threshold=100 -flv-function-specialization
-mllvm -enable-licm-vrp -mllvm -reroll-loops
-mllvm -aggressive-loop-unswitch
-mllvm -reduce-array-computations=3
-mllvm -global-vectorize-slp=true
-mllvm -do-block-reorder=aggressive
-fvirtual-function-elimination -fvisibility=hidden
-lamdlibm -ljemalloc

531.deepsjeng_r: basepeak = yes

(Continued on next page)
Cisco Systems
Cisco UCS C225 M6 (AMD EPYC 7643 48-Core Processor)

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Peak Optimization Flags (Continued)

541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:
548.exchange2_r: basepeak = yes

Peak Other Flags

C benchmarks (except as noted below):
-Wno-unused-command-line-argument

502.gcc_r: -L/usr/lib -Wno-unused-command-line-argument
-L/sppo/bin/cpu2017v115aocc3/amd_rate_aocc300_milan_A_lib/32

C++ benchmarks (except as noted below):
-Wno-unused-command-line-argument

523.xalancbmk_r: -L/usr/lib -Wno-unused-command-line-argument
-L/sppo/bin/cpu2017v115aocc3/amd_rate_aocc300_milan_A_lib/32

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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