Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 5320T, 2.30GHz)

<table>
<thead>
<tr>
<th>Software</th>
<th>SPECrate®2017_fp_base = 295</th>
<th>SPECrate®2017_fp_peak = 296</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU2017 License:</td>
<td>9019</td>
<td>Test Date: Sep-2021</td>
</tr>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
<td>Hardware Availability: Apr-2021</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
<td>Software Availability: Dec-2020</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Hardware</th>
<th>SPECrate®2017_fp_base (295)</th>
<th>SPECrate®2017_fp_peak (296)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Name:</td>
<td>Intel Xeon Gold 5320T</td>
<td></td>
</tr>
<tr>
<td>Max MHz:</td>
<td>3500</td>
<td></td>
</tr>
<tr>
<td>Nominal:</td>
<td>2300</td>
<td></td>
</tr>
<tr>
<td>Enabled:</td>
<td>40 cores, 2 chips, 2 threads/core</td>
<td></td>
</tr>
<tr>
<td>Orderable:</td>
<td>1,2 Chips</td>
<td></td>
</tr>
<tr>
<td>Cache L1:</td>
<td>32 KB I + 48 KB D on chip per core</td>
<td></td>
</tr>
<tr>
<td>Cache L2:</td>
<td>1.25 MB I+D on chip per core</td>
<td></td>
</tr>
<tr>
<td>Cache L3:</td>
<td>30 MB I+D on chip per chip</td>
<td></td>
</tr>
<tr>
<td>Other:</td>
<td>None</td>
<td></td>
</tr>
<tr>
<td>Memory:</td>
<td>1 TB (32 x 32 GB 2Rx4 PC4-3200V-R, running at 2933)</td>
<td></td>
</tr>
<tr>
<td>Storage:</td>
<td>1 x 960 GB M.2 SSD SATA</td>
<td></td>
</tr>
<tr>
<td>Other:</td>
<td>None</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Software</th>
<th>SPECrate®2017_fp_base (295)</th>
<th>SPECrate®2017_fp_peak (296)</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS:</td>
<td>SUSE Linux Enterprise Server 15 SP2</td>
<td>5.3.18-22-default</td>
</tr>
<tr>
<td>Compiler:</td>
<td>C/C++: Version 2021.1 of Intel oneAPI DPC++/C++</td>
<td>Compiler Build 20201113 for Linux; Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux;</td>
</tr>
<tr>
<td>Firmware:</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td>File System:</td>
<td>btrfs</td>
<td></td>
</tr>
<tr>
<td>System State:</td>
<td>Run level 3 (multi-user)</td>
<td></td>
</tr>
<tr>
<td>Base Pointers:</td>
<td>64-bit</td>
<td></td>
</tr>
<tr>
<td>Peak Pointers:</td>
<td>64-bit</td>
<td></td>
</tr>
<tr>
<td>Other:</td>
<td>jemalloc memory allocator V5.0.1</td>
<td></td>
</tr>
<tr>
<td>Power Management:</td>
<td>BIOS and OS set to prefer performance at the cost of additional power usage</td>
<td></td>
</tr>
</tbody>
</table>
**Results Table**

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>80</td>
<td>1247</td>
<td>643</td>
<td>1243</td>
<td>645</td>
<td>1243</td>
<td>645</td>
<td>80</td>
<td>1245</td>
<td>644</td>
<td>1244</td>
<td>645</td>
<td>1246</td>
<td>644</td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>80</td>
<td>255</td>
<td>397</td>
<td>256</td>
<td>396</td>
<td>256</td>
<td>396</td>
<td>80</td>
<td>255</td>
<td>397</td>
<td>256</td>
<td>395</td>
<td>256</td>
<td>396</td>
</tr>
<tr>
<td>508.namd_r</td>
<td>80</td>
<td>360</td>
<td>211</td>
<td>359</td>
<td>212</td>
<td>361</td>
<td>210</td>
<td>80</td>
<td>360</td>
<td>211</td>
<td>359</td>
<td>212</td>
<td>361</td>
<td>210</td>
</tr>
<tr>
<td>510.parest_r</td>
<td>80</td>
<td>1241</td>
<td>169</td>
<td>1241</td>
<td>169</td>
<td>1249</td>
<td>168</td>
<td>80</td>
<td>1244</td>
<td>168</td>
<td>1244</td>
<td>168</td>
<td>1245</td>
<td>168</td>
</tr>
<tr>
<td>511.povray_r</td>
<td>80</td>
<td>585</td>
<td>319</td>
<td>587</td>
<td>318</td>
<td>586</td>
<td>319</td>
<td>80</td>
<td>512</td>
<td>365</td>
<td>515</td>
<td>362</td>
<td>517</td>
<td>361</td>
</tr>
<tr>
<td>519.lbm_r</td>
<td>80</td>
<td>477</td>
<td>177</td>
<td>480</td>
<td>176</td>
<td>480</td>
<td>176</td>
<td>80</td>
<td>477</td>
<td>177</td>
<td>480</td>
<td>175</td>
<td>480</td>
<td>176</td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>80</td>
<td>614</td>
<td>292</td>
<td>616</td>
<td>291</td>
<td>611</td>
<td>293</td>
<td>80</td>
<td>652</td>
<td>275</td>
<td>666</td>
<td>269</td>
<td>660</td>
<td>271</td>
</tr>
<tr>
<td>526.blender_r</td>
<td>80</td>
<td>414</td>
<td>294</td>
<td>413</td>
<td>295</td>
<td>414</td>
<td>294</td>
<td>80</td>
<td>414</td>
<td>294</td>
<td>413</td>
<td>295</td>
<td>414</td>
<td>294</td>
</tr>
<tr>
<td>527.cam4_r</td>
<td>80</td>
<td>469</td>
<td>298</td>
<td>468</td>
<td>299</td>
<td>468</td>
<td>299</td>
<td>80</td>
<td>469</td>
<td>298</td>
<td>468</td>
<td>299</td>
<td>468</td>
<td>299</td>
</tr>
<tr>
<td>538.imagick_r</td>
<td>80</td>
<td>269</td>
<td>740</td>
<td>270</td>
<td>737</td>
<td>268</td>
<td>741</td>
<td>80</td>
<td>269</td>
<td>740</td>
<td>270</td>
<td>737</td>
<td>268</td>
<td>741</td>
</tr>
<tr>
<td>544.nab_r</td>
<td>80</td>
<td>279</td>
<td>482</td>
<td>280</td>
<td>480</td>
<td>278</td>
<td>484</td>
<td>80</td>
<td>274</td>
<td>491</td>
<td>273</td>
<td>493</td>
<td>274</td>
<td>492</td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
<td>80</td>
<td>1542</td>
<td>202</td>
<td>1539</td>
<td>203</td>
<td>1542</td>
<td>202</td>
<td>80</td>
<td>1542</td>
<td>202</td>
<td>1539</td>
<td>203</td>
<td>1542</td>
<td>202</td>
</tr>
<tr>
<td>554.roms_r</td>
<td>80</td>
<td>953</td>
<td>133</td>
<td>950</td>
<td>134</td>
<td>953</td>
<td>133</td>
<td>80</td>
<td>951</td>
<td>134</td>
<td>952</td>
<td>133</td>
<td>950</td>
<td>134</td>
</tr>
</tbody>
</table>

**Submit Notes**

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

**Operating System Notes**

Stack size set to unlimited using "ulimit -s unlimited"

**Environment Variables Notes**

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOC_CONF = "retain:true"

**General Notes**

Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM
memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 5320T, 2.30GHz)  
SPECrate®2017_fp_base = 295  
SPECrate®2017_fp_peak = 296

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Test Date:</td>
<td>Sep-2021</td>
</tr>
<tr>
<td>Hardware Availability:</td>
<td>Apr-2021</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>Dec-2020</td>
</tr>
</tbody>
</table>

General Notes (Continued)

```
sync; echo 3>       /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
```
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
UPI Link Enablement set to 1
UPI Power Management set to Enabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDCS Sparing set to Disabled
Patrol Scrub set to Disabled
Enhanced CPU performance set to Auto
Energy Efficient Turbo set to Enabled
Processor C6 Report set to Enabled
Processor C1E set to Enabled

```
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d
running on localhost Mon Sep  6 18:23:14 2021
```
SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
```
model name : Intel(R) Xeon(R) Gold 5320T CPU @ 2.30GHz
  2  "physical id"s (chips)
  80 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 20
siblings : 40
```

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 5320T, 2.30GHz)

SPEC CPU®2017 Floating Point Rate Result

| SPEC®2017_fp_base = 295 |
| SPEC®2017_fp_peak = 296 |

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Sep-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Platform Notes (Continued)

From lscpu from util-linux 2.33.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 80
On-line CPU(s) list: 0-79
Thread(s) per core: 2
Core(s) per socket: 20
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Gold 5320T CPU @ 2.30GHz
Stepping: 6
CPU MHz: 1253.672
CPU max MHz: 3500.0000
CPU min MHz: 800.0000
BogoMIPS: 4600.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 30720K
NUMA node0 CPU(s): 0-9,40-49
NUMA node1 CPU(s): 10-19,50-59
NUMA node2 CPU(s): 20-29,60-69
NUMA node3 CPU(s): 30-39,70-79

Flags: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dtes64 monitor ds_cpl vmx smx est tm mbe syscall nx pdm dtes64bicmp mcmov popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invpcid_single ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vmi flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha ni avx512bw avx512vl xsaves opt xsaves xgetbv1 xsavec qmx cqm lrc cqm_mbm_total cqm_mbm_local wbnoinvd dtherm ida arat pln pts hwp_act_window hwp epp hwp_pkg_req avx512v bmi umip pku ospke avx512 v bmi2 gfsi vaes vpcmldq avx512_vnni avx512 bitalg tme avx512_vp opcnt dq la57 rdrid md_clear pconfig flush lld arch_capabilities

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 5320T, 2.30GHz)

Platform Notes (Continued)

/proc/cpuinfo cache data
  cache size : 30720 KB

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 4 nodes (0-3)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 40 41 42 43 44 45 46 47 48 49
  node 0 size: 257636 MB
  node 0 free: 257063 MB
  node 1 cpus: 10 11 12 13 14 15 16 17 18 19 50 51 52 53 54 55 56 57 58 59
  node 1 size: 258043 MB
  node 1 free: 257704 MB
  node 2 cpus: 20 21 22 23 24 25 26 27 28 29 60 61 62 63 64 65 66 67 68 69
  node 2 size: 258043 MB
  node 2 free: 257776 MB
  node 3 cpus: 30 31 32 33 34 35 36 37 38 39 70 71 72 73 74 75 76 77 78 79
  node 3 size: 258005 MB
  node 3 free: 257748 MB
  node distances:
    node   0   1   2   3
    0:  10  11  20  20
    1:  11  10  20  20
    2:  20  20  10  11
    3:  20  20  11  10

From /proc/meminfo
  MemTotal: 1056489636 kB
  HugePages_Total: 0
  Hugepagesize: 2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15-SP2"
    VERSION_ID="15.2"
    PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15:sp2"

  uname -a:
    Linux localhost 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
    x86_64 x86_64 GNU/Linux

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 5320T, 2.30GHz)

| SPECrate®2017_fp_base = 295 |
| SPECrate®2017_fp_peak = 296 |

**CPU2017 License:** 9019
**Test Sponsor:** Cisco Systems
**Tested by:** Cisco Systems

**Platform Notes (Continued)**

Kernel self-reported vulnerability status:

- **CVE-2018-12207 (iTLB Multihit):** Not affected
- **CVE-2018-3620 (L1 Terminal Fault):** Not affected
- **Microarchitectural Data Sampling:** Not affected
- **CVE-2017-5754 (Meltdown):** Mitigation: Speculative Store Bypass disabled via prctl and seccomp
- **CVE-2018-3639 (Speculative Store Bypass):** Mitigation: usercopy/swapgs barriers and __user pointer sanitization
- **CVE-2017-5753 (Spectre variant 1):** Mitigation: usercopy/swapgs barriers and __user pointer sanitization
- **CVE-2017-5715 (Spectre variant 2):** Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
- **CVE-2020-0543 (Special Register Buffer Data Sampling):** Not affected
- **CVE-2019-11135 (TSX Asynchronous Abort):** Not affected

**run-level 3 Sep 6 17:56**

**SPEC is set to:** /home/cpu2017

```
Filesystem   Type      Size  Used Avail Use% Mounted on
/dev/sdb2      btrfs  222G   33G  189G  15% /home
```

From /sys/devices/virtual/dmi/id

- **Vendor:** Cisco Systems Inc
- **Product:** UCSC-C220-M6S
- **Serial:** WZP244104TF

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

- **Memory:**
  - 32x 0xCE00 M393A4K40DB3-CWE 32 GB 2 rank 3200, configured at 2933

**BIOS:**

- **BIOS Vendor:** Cisco Systems, Inc.
- **BIOS Version:** C220M6.4.2.1d.0.0730210924
- **BIOS Date:** 07/30/2021
- **BIOS Revision:** 5.22

(End of data from sysinfo program)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 5320T, 2.30GHz)

SPECraten®2017_fp_base = 295
SPECraten®2017_fp_peak = 296

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Sep-2021
Tested by: Cisco Systems
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Compiler Version Notes

==============================================================================
C               | 519.lbm_r(base, peak) 538.imagick_r(base, peak)
                 | 544.nab_r(base, peak)
==============================================================================
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================
C++             | 508.namd_r(base, peak) 510.parest_r(base, peak)
==============================================================================
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================
C++, C          | 511.povray_r(peak)
==============================================================================
Intel(R) C++ Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================
C++, C          | 511.povray_r(base) 526.blender_r(base, peak)
==============================================================================
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 5320T, 2.30GHz)

SPECrater®2017_fp_base = 295
SPECrater®2017_fp_peak = 296

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Sep-2021
Hardware Availability: Apr-2021
Tested by: Cisco Systems
Software Availability: Dec-2020

Compiler Version Notes (Continued)

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================
C++, C          | 511.povray_r(base) 526.blender_r(base, peak)
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================
C++, C, Fortran | 507.cactuBSSN_r(base, peak)
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================
Fortran         | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
                  | 554.roms_r(base, peak)
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================
Fortran, C      | 521.wrf_r(peak)
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 5320T, 2.30GHz)

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
<th>Test Date:</th>
<th>Sep-2021</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
<td>Hardware Availability:</td>
<td>Apr-2021</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
<td>Software Availability:</td>
<td>Dec-2020</td>
</tr>
</tbody>
</table>

**SPECrate®2017_fp_base = 295**  
**SPECrate®2017_fp_peak = 296**

### Compiler Version Notes (Continued)

<table>
<thead>
<tr>
<th>Compiler invocation</th>
<th>Fortran, C</th>
<th>521.wrf_r(base) 527.cam4_r(base, peak)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Copyright (C) 1985-2020 Intel Corporation. All rights reserved.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Compiler invocation</th>
<th>Fortran, C</th>
<th>521.wrf_r(peak)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Copyright (C) 1985-2020 Intel Corporation. All rights reserved.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Base Compiler Invocation

C benchmarks:
- icx

C++ benchmarks:
- icpx

Fortran benchmarks:
- ifort

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 5320T, 2.30GHz)

SPECrater®2017_fp_base = 295
SPECrater®2017_fp_peak = 296

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Sep-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Base Compiler Invocation (Continued)

Benchmarks using both Fortran and C:
ifort icx

Benchmarks using both C and C++:
icpx icx

Benchmarks using Fortran, C, and C++:
icpx icx ifort

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

C++ benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Fortran benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -03 -ipo -no-prec-div
-qopt-prefetch -ffinite-math-only

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 5320T, 2.30GHz)

SPECrate®2017_fp_base = 295
SPECrate®2017_fp_peak = 296

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Sep-2021
Hardware Availability: Apr-2021
Tested by: Cisco Systems
Software Availability: Dec-2020

Base Optimization Flags (Continued)

Fortran benchmarks (continued):
-qopt-multiple-gather-scatter-by-shuffles -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto
-mbranches-within-32B-boundaries -ljemalloc
-\L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using both Fortran and C:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-align array32byte -auto -ljemalloc -\L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using both C and C++:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-\L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using Fortran, C, and C++:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-align array32byte -auto -ljemalloc -\L/usr/local/jemalloc64-5.0.1/lib

Peak Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
521.wrf_r: ifort icc

(Continued on next page)
### Peak Compiler Invocation (Continued)

527.cam4_r: ifort icx

Benchmarks using both C and C++:

511.povray_r: icpc icc
526.blender_r: icpx icx

Benchmarks using Fortran, C, and C++:

icpx icx ifort

### Peak Portability Flags

Same as Base Portability Flags

### Peak Optimization Flags

#### C benchmarks:

519.lbm_r: basepeak = yes
538.imagick_r: basepeak = yes

544.nab_r: -w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -flto
-Ofast -qopt-mem-layout-trans=4
-fimf-accuracy-bits=14:sqrt
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

#### C++ benchmarks:

508.namd_r: basepeak = yes

510.parest_r: -w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

#### Fortran benchmarks:

503.bwaves_r: -w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 5320T, 2.30GHz)

SPECrate®2017_fp_base = 295
SPECrate®2017_fp_peak = 296

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Sep-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Peak Optimization Flags (Continued)

503.bwaves_r (continued):
-`qopt-multiple-gather-scatter-by-shuffles`
-`qopt-mem-layout-trans=4 -nostandard-realloc-lhs`
-`align array32byte -auto -mbranches-within-32B-boundaries`
-`ljemalloc -L/usr/local/jemalloc64-5.0.1/lib`

549.fotonik3d_r: basepeak = yes

554.roms_r: Same as 503.bwaves_r

Benchmarks using both Fortran and C:

521.wrf_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3
-ipo -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-nostandard-realloc-lhs -align array32byte -auto
-`L/usr/local/jemalloc64-5.0.1/lib -ljemalloc`

527.cam4_r: basepeak = yes

Benchmarks using both C and C++:

511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3
-ipo -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-`L/usr/local/jemalloc64-5.0.1/lib -ljemalloc`

526.blender_r: basepeak = yes

Benchmarks using Fortran, C, and C++:

507.cactuBSSN_r: basepeak = yes

The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:

http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 5320T, 2.30GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base = 295</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_fp_peak = 296</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU2017 License:</td>
<td>9019</td>
</tr>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
</tbody>
</table>

Test Date: Sep-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.8 on 2021-09-06 21:23:13-0400.
Report generated on 2021-09-29 12:31:34 by CPU2017 PDF formatter v6442.
Originally published on 2021-09-28.