Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 5320T, 2.30GHz)

SPECspeed®2017_fp_base = 164
SPECspeed®2017_fp_peak = 165

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Threads

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<tr>
<th>SPECspeed®2017_fp_base (164)</th>
<th>SPECspeed®2017_fp_peak (165)</th>
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<tr>
<td>603.bwaves_s 40</td>
<td>612</td>
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<tr>
<td>607.cactuBSSN_s 40</td>
<td></td>
</tr>
<tr>
<td>619.lbm_s 40</td>
<td>123</td>
</tr>
<tr>
<td>621.wrf_s 40</td>
<td>143</td>
</tr>
<tr>
<td>627.cam4_s 40</td>
<td>114</td>
</tr>
<tr>
<td>628.pop2_s 40</td>
<td>77.0</td>
</tr>
<tr>
<td>638.imagick_s 40</td>
<td>164</td>
</tr>
<tr>
<td>644.nab_s 40</td>
<td>276</td>
</tr>
<tr>
<td>649.fotonik3d_s 40</td>
<td>98.4</td>
</tr>
<tr>
<td>654.roms_s 40</td>
<td>165</td>
</tr>
</tbody>
</table>

Hardware

CPU Name: Intel Xeon Gold 5320T
Max MHz: 3500
Nominal: 2300
Enabled: 40 cores, 2 chips
Orderable: 1.2 Chips
Cache L1: 32 KB I + 48 KB D on chip per core
L2: 1.25 MB I+D on chip per core
L3: 30 MB I+D on chip per chip
Other: None
Memory: 1 TB (32 x 32 GB 2Rx4 PC4-3200V-R, running at 2933)
Storage: 1 x 960 GB M.2 SSD SATA
Other: None

Software

OS: SUSE Linux Enterprise Server 15 SP2 5.3.18-22-default
Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux;
           Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux;
Parallel: Yes
Firmware: Version 4.2.1d released Jul-2021
File System: btrfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS and OS set to prefer performance at the cost of additional power usage
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 5320T, 2.30GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Results Table

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<tr>
<th>Benchmark</th>
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<th>Ratio</th>
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<tr>
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<td>151</td>
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<tr>
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<td>77.0</td>
<td>119</td>
<td>77.6</td>
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<td>77.6</td>
<td>114</td>
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<tr>
<td>628.pop2_s</td>
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<tr>
<td>638.imagick_s</td>
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<td>87.7</td>
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<td>165</td>
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<td>164</td>
</tr>
<tr>
<td>644.nab_s</td>
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<td>63.2</td>
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<td>63.2</td>
<td>276</td>
<td>64.1</td>
<td>273</td>
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<tr>
<td>649.fotonik3d_s</td>
<td>40</td>
<td>92.7</td>
<td>150</td>
<td>93.0</td>
<td>98.0</td>
<td>91.9</td>
<td>99.2</td>
<td>92.8</td>
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<td>654.roms_s</td>
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<td>165</td>
<td>95.3</td>
<td>165</td>
<td>95.3</td>
<td>165</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOC_CONF = "retain:true"
OMP_STACKSIZE = "192M"

General Notes

Binsaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM memory using Redhat Enterprise Linux 8.0
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 5320T, 2.30GHz)

<table>
<thead>
<tr>
<th>SPECspeed®2017_fp_base = 164</th>
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</thead>
<tbody>
<tr>
<td>SPECspeed®2017_fp_peak = 165</td>
</tr>
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</table>

CPU2017 License: 9019  Test Date: Sep-2021
Test Sponsor: Cisco Systems  Hardware Availability: Apr-2021
Tested by: Cisco Systems  Software Availability: Dec-2020

General Notes (Continued)

Platform Notes

BIOS Settings:
Intel Hyper-Threading Technology set to Disabled
DCU Streamer Prefetch set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDDC Sparing set to Disabled
Patrol Scrub set to Disabled
Energy Efficient Turbo set to Enabled
Processor C6 Report set to Enabled
Processor C1E set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d
running on localhost Thu Sep 2 20:26:37 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 5320T CPU @ 2.30GHz
  2 "physical id"s (chips)
  40 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 20
  siblings : 20
  physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
  physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19

From lscpu from util-linux 2.33.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 40
On-line CPU(s) list: 0-39
Thread(s) per core: 1
Core(s) per socket: 20
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 5320T, 2.30GHz)

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SPECspeed®2017_fp_base = 164
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Test Date: Sep-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Platform Notes (Continued)

Model: 106
Model name: Intel(R) Xeon(R) Gold 5320T CPU @ 2.30GHz
Stepping: 6
CPU MHz: 1351.226
CPU max MHz: 3500.0000
CPU min MHz: 800.0000
BogoMIPS: 4600.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 30720K
NUMA node0 CPU(s): 0-19
NUMA node1 CPU(s): 20-39
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmonperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 invpcid_single ssbd
mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vmmi flexpriority ept vpid ept_ad
fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cmp rdt_a avx512f
avx512dq rdseedadx smap avx512ifma clflushopt clwb intel_pt avx512cd sha ni
avx512bw avx512vl xsaves opt xsaves xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total
cqm_mbm_local wboinvd dtherm ida arat pln pts hwp hwp_act_window hwp_epp
hwp_pkg_req avx512bvmi umip pku ospke avx512_vbmi2 qnri vaes vpcmldqdq avx512 vnvl
avx512_bitalg tme avx512_vpopcntdq la57 rdpid md_clear pconfig flush_lid
arch_capabilities

/proc/cpuinfo cache data
  cache size : 30720 KB

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
node 0 size: 515683 MB
node 0 free: 511753 MB
node 1 cpus: 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39
node 1 size: 516054 MB
node 1 free: 514848 MB
node distances:
  node 0 1
    0: 10 20
    1: 20 10

From /proc/meminfo

(Continued on next page)
Cisco Systems
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SPECspeed®2017_fp_base = 164
SPECspeed®2017_fp_peak = 165

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

MemTotal: 1056499796 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15-SP2"
    VERSION_ID="15.2"
    PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
  Linux localhost 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
  x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swaps barriers and __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Sep 2 17:54

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sdb2 btrfs 222G 36G 186G 17% /home

From /sys/devices/virtual/dmi/id
  Vendor: Cisco Systems Inc

(Continued on next page)
Cisco Systems
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Sep-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Platform Notes (Continued)

Product: UCSC-C220-M6S
Serial: WZP244104TF

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
32x 0xCE00 M393A4K40DB3-CWE 32 GB 2 rank 3200, configured at 2933

BIOS:
 BIOS Vendor: Cisco Systems, Inc.
 BIOS Version: C220M6.4.2.1d.0.0730210924
 BIOS Date: 07/30/2021
 BIOS Revision: 5.22

(End of data from sysinfo program)

Compiler Version Notes

=================================================================================
<table>
<thead>
<tr>
<th>C</th>
<th>619.lbm_s(base, peak) 638.imagick_s(base, peak)</th>
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<tbody>
<tr>
<td></td>
<td>644.nab_s(base)</td>
</tr>
</tbody>
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=================================================================================

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=================================================================================
| C               | 644.nab_s(peak)                              |
=================================================================================

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

=================================================================================
<table>
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Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Cisco Systems

Cisco UCS C220 M6 (Intel Xeon Gold 5320T, 2.30GHz)

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CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems

Test Date: Sep-2021  
Hardware Availability: Apr-2021  
Software Availability: Dec-2020

### Compiler Version Notes (Continued)

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| Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
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<tr>
<td>C++, C, Fortran</td>
<td>607.cactuBSSN_s(base, peak)</td>
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<td>-----------------</td>
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| Intel(R) C++ Intel(R) 64 Compiler Classic for applications running on  
  Intel(R) 64, Version 2021.1 Build 20201112_000000  
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Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)  
64, Version 2021.1 Build 20201112_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on  
Intel(R) 64, Version 2021.1 Build 20201112_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved. |
|-----------------|-----------------|
| Fortran         | 603.bwaves_s(base, peak) 649.fotonik3d_s(base, peak)  
  654.roms_s(base, peak) |
|-----------------|-----------------|
| Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on  
  Intel(R) 64, Version 2021.1 Build 20201112_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved. |
|-----------------|-----------------|
| Fortran, C      | 621.wrf_s(base, peak) 627.cam4_s(base, peak)  
  628.pop2_s(base, peak) |
|-----------------|-----------------|
| Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on  
  Intel(R) 64, Version 2021.1 Build 20201112_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)  
64, Version 2021.1 Build 20201112_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved. |
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Base Compiler Invocation

C benchmarks:
icc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-m64 -std=c11 -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-mbranches-within-32B-boundaries

Fortran benchmarks:
-m64 -Wl,-z,muldefs -DSPEC_OPENMP -xCORE-AVX2 -ipo -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-nostandard-realloc-lhs -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Benchmarks using both Fortran and C:
-m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX2 -ipo -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 5320T, 2.30GHz)  

SPECspeed®2017_fp_base = 164
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Test Sponsor: Cisco Systems
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Test Date: Sep-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Base Optimization Flags (Continued)

Benchmarks using both Fortran and C (continued):
-DSPEC_OPENMP -mbranches-within-32B-boundaries -nostandard-realloc-lhs
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Benchmarks using Fortran, C, and C++:
-m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX2 -ipo -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-DSPEC_OPENMP -mbranches-within-32B-boundaries -nostandard-realloc-lhs
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Peak Compiler Invocation

C benchmarks (except as noted below):
icc

644.nab_s: icx

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
619.lbm_s: basepeak = yes
638.imagick_s: basepeak = yes
644.nab_s: -m64 -Wl,-z,muldefs -xCORE-AVX2 -Ofast -ffast-math
-mfpmath=sse -funroll-loops -fiopenmp

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 5320T, 2.30GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Peak Optimization Flags (Continued)

644.nab_s (continued):
-DSPEC_OPENMP -qopt-mem-layout-trans=4
-fimf-accuracy-bits=14:sqrt
-mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Fortran benchmarks:

603.bwaves_s: -m64 -Wl,-z,muldefs -prof-gen(pass l) -prof-use(pass 2)
-DSPEC_SUPPRESS_OPENMP -DSPEC_OPENMP -ipo -xCORE-AVX2
-03 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -qopenmp -nostandard-realloc-lhs
-mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

649.fotonik3d_s: Same as 603.bwaves_s

654.roms_s: basepeak = yes

Benchmarks using both Fortran and C:

621.wrf_s: -m64 -std=c11 -Wl,-z,muldefs -prof-gen(pass l)
-prof-use(pass 2) -ipo -xCORE-AVX2 -03 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

627.cam4_s: basepeak = yes

628.pop2_s: basepeak = yes

Benchmarks using Fortran, C, and C++:

607.cactusBSSN_s: basepeak = yes

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 5320T, 2.30GHz)

SPECspeed®2017_fp_base = 164
SPECspeed®2017_fp_peak = 165

CPU2017 License: 9019
Test Sponsor: Cisco Systems
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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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