# SPEC CPU® 2017 Floating Point Rate Result

## Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Silver 4310T, 2.30GHz)

### SPECrate® 2017 fp_base = 168

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>SPECrate® 2017_fp_peak</th>
<th>SPECrate® 2017_fp_base</th>
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<tr>
<td>503.bwaves_r</td>
<td>40</td>
<td>215</td>
<td>168</td>
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<tr>
<td>507.cactuBSSN_r</td>
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<tr>
<td>538.imagick_r</td>
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**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Test Date:** Sep-2021  
**Hardware Availability:** Apr-2021  
**Software Availability:** Dec-2020

### Hardware

- **CPU Name:** Intel Xeon Silver 4310T  
- **Max MHz:** 3400  
- **Nominal:** 2300  
- **Enabled:** 20 cores, 2 chips, 2 threads/core  
- **Orderable:** 1,2 Chips  
- **Cache L1:** 32 KB I + 48 KB D on chip per core  
- **L2:** 1.25 MB I+D on chip per core  
- **L3:** 15 MB I+D on chip per core  
- **Other:** None  
- **Memory:** 1 TB (32 x 32 GB 2Rx4 PC4-3200V-R, running at 2666)  
- **Storage:** 1 x 960 GB M.2 SSD SATA  
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 15 SP2  
  5.3.18-22-default  
- **Compiler:** C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux;  
  Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux;  
- **Parallel:** No  
- **Firmware:** Version 4.2.1d released Jul-2021  
- **File System:** btrfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** 64-bit  
- **Power Management:** BIOS and OS set to prefer performance at the cost of additional power usage
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Silver 4310T, 2.30GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Results Table

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**Submit Notes**

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

**Operating System Notes**

Stack size set to unlimited using "ulimit -s unlimited"

**Environment Variables Notes**

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOC_CONF = "retain:true"

**General Notes**

Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM
memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Silver 4310T, 2.30GHz)

**SPECrate®2017_fp_base = 168**
**SPECrate®2017_fp_peak = 169**

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<th>Test Date:</th>
<th>Sep-2021</th>
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<td>Hardware Availability:</td>
<td>Apr-2021</td>
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<td>Cisco Systems</td>
<td>Software Availability:</td>
<td>Dec-2020</td>
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### General Notes (Continued)

```plaintext
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
```

### Platform Notes

**BIOS Settings:**
- Adjacent Cache Line Prefetcher set to Disabled
- DCU Streamer Prefetch set to Disabled
- UPI Link Enablement set to 1
- UPI Power Management set to Enabled
- Sub NUMA Clustering set to Enabled
- LLC Dead Line set to Disabled
- Memory Refresh Rate set to 1x Refresh
- ADDDC Sparing set to Disabled
- Patrol Scrub set to Disabled
- Enhanced CPU performance set to Auto
- Energy Efficient Turbo set to Enabled
- Processor C6 Report set to Enabled
- Processor C1E set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acfc64d
running on localhost Mon Sep 13 19:15:50 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4310T CPU @ 2.30GHz
  2 "physical id"s (chips)
  40 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 10
siblings : 20
physical 0: cores 0 1 2 3 4 5 6 7 8 9

(Continued on next page)
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### Platform Notes (Continued)

```plaintext
physical 1: cores 0 1 2 3 4 5 6 7 8 9

From lscpu from util-linux 2.33.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 40
On-line CPU(s) list: 0-39
Thread(s) per core: 2
Core(s) per socket: 10
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Silver 4310T CPU @ 2.30GHz
Stepping: 6
CPU MHz: 828.637
CPU max MHz: 3400.0000
CPU min MHz: 800.0000
BogoMIPS: 4600.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 15360K
NUMA node0 CPU(s): 0-9,20-29
NUMA node1 CPU(s): 10-19,30-39
Flags: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invpcid_single ssbd mba ibrs ibpb ibrs_enhanced tpr_shadow vmni flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 3msc emms invpcid rtm cqm rdt_a avx512f avx512dq rseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha ni athx avx512bw avx512vl xsaveopt xsavec xgetbv1 xsavev cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local wboinvd dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_kkg_req avx512vbm  umip pku ospke avx512_vbmi2 gfnl vaes vpclmulqdq avx512_vnni avx512_vbitalg tme avx512 vpoptdqv bga57 rdpid md_clear pconfig flush_lid arch_capabilities

/proc/cpuinfo cache data
  cache size : 15360 KB
```

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Silver 4310T, 2.30GHz)

SPECrate®2017_fp_base = 168
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Platform Notes (Continued)

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
    available: 2 nodes (0-1)
        node 0 cpus: 0 1 2 3 4 5 6 7 8 9 20 21 22 23 24 25 26 27 28 29
        node 0 size: 515683 MB
        node 0 free: 515120 MB
        node 1 cpus: 10 11 12 13 14 15 16 17 18 19 30 31 32 33 34 35 36 37 38 39
        node 1 size: 516054 MB
        node 1 free: 515487 MB
        node distances:
        node 0 1
        0: 10 20
        1: 20 10

From /proc/meminfo
    MemTotal: 1056499796 kB
    HugePages_Total: 0
    Hugepagesize: 2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
    os-release:
        NAME="SLES"
        VERSION="15-SP2"
        VERSION_ID="15.2"
        PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
        ID="sles"
        ID_LIKE="suse"
        ANSI_COLOR=0;32"
        CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
    Linux localhost 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
    x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs

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Cisco Systems
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Platform Notes (Continued)

barriers and __user pointer sanitization
Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

CVE-2017-5715 (Spectre variant 2):

CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Sep 13 19:04

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sdb2 btrfs 222G 33G 189G 15% /home

From /sys/devices/virtual/dmi/id
Vendor: Cisco Systems Inc
Product: UCSC-C220-M6S
Serial: WZP244104TF

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
32x 0xCE00 M393A4K40DB3-CWE 32 GB 2 rank 3200, configured at 2666

BIOS:
BIOS Vendor: Cisco Systems, Inc.
BIOS Version: C220M6.4.2.id.0.0730210924
BIOS Date: 07/30/2021
BIOS Revision: 5.22

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C | 519.lbm_r(base, peak) 538.imagick_r(base, peak)
   544.nab_r(base, peak)
==============================================================================

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================
C++ | 508.namd_r(base, peak) 510.parest_r(base, peak)
(Continued on next page)
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Compiler Version Notes (Continued)

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C++, C, Fortran | 507.cactuBSSN_r(base, peak)
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==============================================================================
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================
Fortran, C | 521.wrf_r(base) 527.cam4_r(base, peak)
==============================================================================
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
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==============================================================================

Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icx

Benchmarks using both C and C++:
icpx icx

Benchmarks using Fortran, C, and C++:
icpx icx ifort
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Silver 4310T, 2.30GHz)

**SPECrate®2017_fp_base = 168**
**SPECrate®2017_fp_peak = 169**

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**Base Portability Flags**

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

**Base Optimization Flags**

C benchmarks:
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

C++ benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

Fortran benchmarks:

Benchmarks using both Fortran and C:

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Silver 4310T, 2.30GHz)

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<td>Tested by: Cisco Systems</td>
<td>Software Availability: Dec-2020</td>
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### Base Optimization Flags (Continued)

Benchmarks using both C and C++:
```
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib
```

Benchmarks using Fortran, C, and C++:
```
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib
```

### Peak Compiler Invocation

**C benchmarks:**
```
icx
```

**C++ benchmarks:**
```
icpx
```

**Fortran benchmarks:**
```
ifort
```

Benchmarks using both Fortran and C:
```
521.wrf_r:ifort icc
527.cam4_r:ifort icx
```

Benchmarks using both C and C++:
```
511.povray_r:icpc icc
526.blender_r:icpx icx
```

Benchmarks using Fortran, C, and C++:
```
icpx icx ifort
```

---

Page 11 Standard Performance Evaluation Corporation (info@spec.org) https://www.spec.org/
## SPEC CPU®2017 Floating Point Rate Result

**Cisco Systems**  
Cisco UCS C220 M6 (Intel Xeon Silver 4310T, 2.30GHz)  

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**Test Sponsor:** Cisco Systems  
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<td>Software Availability:</td>
<td>Dec-2020</td>
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### Peak Portability Flags

Same as Base Portability Flags

### Peak Optimization Flags

**C benchmarks:**

519.lbm_r: basepeak = yes  
538.imagick_r: basepeak = yes  

**C++ benchmarks:**

508.namd_r: basepeak = yes  

**Fortran benchmarks:**

549.fotonik3d_r: basepeak = yes  
554.roms_r: Same as 503.bwaves_r

**Benchmarks using both Fortran and C:**

521.wrf_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-multiple-gather-scatter-by-shuffles -qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries

(Continued on next page)
Cisco Systems

Cisco UCS C220 M6 (Intel Xeon Silver 4310T, 2.30GHz)

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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Peak Optimization Flags (Continued)

521.wrf_r (continued):
- nostandard-realloc-lhs -align array32byte -auto
- L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

527.cam4_r: basepeak = yes

Benchmarks using both C and C++:

511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3
-ipo -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

526.blender_r: basepeak = yes

Benchmarks using Fortran, C, and C++:

507.cactuBSSN_r: basepeak = yes

The flags files that were used to format this result can be browsed at:

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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