Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6312U, 2.40GHz)

Copyright 2017-2021 Standard Performance Evaluation Corporation

SPECrate®2017_fp_base = 175
SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Sep-2021
Hardware Availability: Apr-2021
Tested by: Cisco Systems
Software Availability: Dec-2020

Hardware
CPU Name: Intel Xeon Gold 6312U
Max MHz: 3600
Nominal: 2400
Enabled: 24 cores, 1 chip, 2 threads/core
Orderable: 1 Chip
Cache L1: 32 KB I + 48 KB D on chip per core
L2: 1.25 MB I+D on chip per core
L3: 36 MB I+D on chip per chip
Other: None
Memory: 512 GB (8 x 64 GB 2Rx4 PC4-3200V-R)
Storage: 1 x 240 GB M.2 SSD SATA
Other: None

Software
OS: SUSE Linux Enterprise Server 15 SP2
5.3.18-22-default
Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++
Compiler Build 20201113 for Linux;
Fortran: Version 2021.1 of Intel Fortran Compiler
Classic Build 20201112 for Linux
Parallel: No
Firmware: Version 4.2.1d released Jul-2021
File System: btrfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS and OS set to prefer performance at the cost of additional power usage
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6312U, 2.40GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECrate®2017_fp_base = 175
SPECrate®2017_fp_peak = Not Run

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>48</td>
<td>1323</td>
<td>364</td>
<td>1323</td>
<td>364</td>
<td>1323</td>
<td>364</td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>48</td>
<td>257</td>
<td>237</td>
<td>258</td>
<td>235</td>
<td>259</td>
<td>235</td>
</tr>
<tr>
<td>508.namd_r</td>
<td>48</td>
<td>356</td>
<td>128</td>
<td>356</td>
<td>128</td>
<td>358</td>
<td>127</td>
</tr>
<tr>
<td>510.parest_r</td>
<td>48</td>
<td>1297</td>
<td>96.8</td>
<td>1297</td>
<td>96.8</td>
<td>1295</td>
<td>96.9</td>
</tr>
<tr>
<td>511.povray_r</td>
<td>48</td>
<td>596</td>
<td>188</td>
<td>595</td>
<td>189</td>
<td>595</td>
<td>188</td>
</tr>
<tr>
<td>519.lbm_r</td>
<td>48</td>
<td>369</td>
<td>137</td>
<td>368</td>
<td>137</td>
<td>369</td>
<td>137</td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>48</td>
<td>464</td>
<td>162</td>
<td>465</td>
<td>164</td>
<td>468</td>
<td>157</td>
</tr>
<tr>
<td>526.blender_r</td>
<td>48</td>
<td>425</td>
<td>172</td>
<td>426</td>
<td>172</td>
<td>425</td>
<td>172</td>
</tr>
<tr>
<td>527.cam4_r</td>
<td>48</td>
<td>487</td>
<td>172</td>
<td>482</td>
<td>174</td>
<td>487</td>
<td>172</td>
</tr>
<tr>
<td>538.imagick_r</td>
<td>48</td>
<td>259</td>
<td>460</td>
<td>260</td>
<td>459</td>
<td>260</td>
<td>460</td>
</tr>
<tr>
<td>544.nab_r</td>
<td>48</td>
<td>281</td>
<td>288</td>
<td>280</td>
<td>288</td>
<td>280</td>
<td>288</td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
<td>48</td>
<td>1698</td>
<td>110</td>
<td>1695</td>
<td>110</td>
<td>1696</td>
<td>110</td>
</tr>
<tr>
<td>554.roms_r</td>
<td>48</td>
<td>1014</td>
<td>75.2</td>
<td>1015</td>
<td>75.1</td>
<td>1011</td>
<td>75.5</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOC_CONF = "retain:true"

General Notes
Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6312U, 2.40GHz)

SPECraten®2017_fp_base = 175
SPECraten®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Sep-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

General Notes (Continued)

sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
Sub NUMA Clustering set to Enabled
Patrol Scrub set to Disabled
Processor C6 Report set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acac64d
running on localhost Thu Sep  9 04:58:15 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6312U CPU @ 2.40GHz
  1 "physical id"s (chips)
  48 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 24
siblings : 48
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23

From lscpu from util-linux 2.33.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6312U, 2.40GHz)

SPEC CPU®2017 Floating Point Rate Result
Copyright 2017-2021 Standard Performance Evaluation Corporation

Platform Notes (Continued)

Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 48
On-line CPU(s) list: 0-47
Thread(s) per core: 2
Core(s) per socket: 24
Socket(s): 1
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Gold 6312U CPU @ 2.40GHz
Stepping: 6
CPU MHz: 3265.412
CPU max MHz: 3600.0000
CPU min MHz: 800.0000
BogoMIPS: 4800.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 36864K
NUMA node0 CPU(s): 0-11,24-35
NUMA node1 CPU(s): 12-23,36-47
Flags: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtrunc pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 invpcid_single ssbd mba ibrs ibpb ibrs Enhanced tpr_shadow vmm赎 priority 1ept gp vpt_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 64bit ripng ipid rtm cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha ni axsvx12bw avx512vl xsaveopt xsavec xsaveprec xsaveav xsavec qcmpml qcmpml local wbnoinvd dtherm ida arat pfn ts hwp hwp_act_window hwp epp hwp_pkg_req avx512bmi umip pku ospke avx512_vbmi2 gfn vaes vpclmulqdq avx512_vnni avx512_vbitalg tme avx512 vpoptndq la57 rdpid md_clear pconfig flush_l1d arch_capabilities

/proc/cpuinfo cache data
  cache size: 36864 KB

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
  available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 24 25 26 27 28 29 30 31 32 33 34 35
node 0 size: 257530 MB
node 0 free: 257134 MB

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6312U, 2.40GHz)

SPECCpu®2017 Floating Point Rate Result
Copyright 2017-2021 Standard Performance Evaluation Corporation

Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6312U, 2.40GHz)

SPECCpu®2017_fp_base = 175
SPECCpu®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

node 1 cpus: 12 13 14 15 16 17 18 19 20 21 22 23 36 37 38 39 40 41 42 43 44 45 46 47
node 1 size: 257762 MB
node 1 free: 257361 MB
node distances:
node 0 1
0: 10 11
1: 11 10

From /proc/meminfo
MemTotal: 527660216 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release*/etc/*version*

os-release:
NAME="SLES"
VERSION="15-SP2"
VERSION_ID="15.2"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
Linux localhost 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit):
Not affected

CVE-2018-3620 (L1 Terminal Fault):
Not affected

Microarchitectural Data Sampling:
Not affected

CVE-2017-5754 (Meltdown):
Not affected

CVE-2018-3639 (Speculative Store Bypass):
Mitigation: Speculative Store Bypass disabled via prctl and seccomp

CVE-2017-5753 (Spectre variant 1):
Mitigation: usercopy/swaps barriers and __user pointer sanitation

CVE-2017-5715 (Spectre variant 2):
Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

CVE-2020-0543 (Special Register Buffer Data Sampling):
Not affected

CVE-2019-11135 (TSX Asynchronous Abort):
Not affected

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6312U, 2.40GHz)

SPECrate®2017_fp_base = 175
SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Sep-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Platform Notes (Continued)

run-level 3 Sep 9 04:57
SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda2 btrfs 222G 9.1G 212G 5% /home

From /sys/devices/virtual/dmi/id
Vendor: Cisco Systems Inc
Product: UCSB-B200-M6
Serial: FCH24097576

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
8x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200
24x NO DIMM NO DIMM

BIOS:
BIOS Vendor: Cisco Systems, Inc.
BIOS Version: B200M6.4.2.id.0.0730210924
BIOS Date: 07/30/2021
BIOS Revision: 5.22

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
| C               | 519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base) |
==============================================================================
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================

==============================================================================
| C++             | 508.namd_r(base) 510.parest_r(base) |
==============================================================================
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6312U, 2.40GHz)  

| SPECrate®2017_fp_base = 175 |

| SPECrate®2017_fp_peak = Not Run |

---

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems  
Test Date: Sep-2021  
Hardware Availability: Apr-2021  
Software Availability: Dec-2020

---

Compiler Version Notes (Continued)

```
C++, C | 511.povray_r(base) 526.blender_r(base)
```

```
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
```

```
C++, C, Fortran | 507.cactuBSSN_r(base)
```

```
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
```

```
Fortran | 503.bwaves_r(base) 549.fotonik3d_r(base) 554.roms_r(base)
```

```
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on  
Intel(R) 64, Version 2021.1 Build 20201112_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
```

```
Fortran, C | 521.wrf_r(base) 527.cam4_r(base)
```

```
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on  
Intel(R) 64, Version 2021.1 Build 20201112_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
```

```
Fortran, C | 521.wrf_r(base) 527.cam4_r(base)
```

```
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on  
Intel(R) 64, Version 2021.1 Build 20201112_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
```

```
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
```
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6312U, 2.40GHz)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6312U, 2.40GHz)

| SPECrate®2017_fp_base = 175 |
| SPECrate®2017_fp_peak = Not Run |

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Sep-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Base Optimization Flags (Continued)

C++ benchmarks:
- -w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -flto
- -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
- -mbranches-within-32B-boundaries -ljemalloc
- -L/usr/local/jemalloc64-5.0.1/lib

Fortran benchmarks:
- -w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
- -qopt-prefetch -ffinite-math-only
- -qopt-multiple-gather-scatter-by-shuffles -qopt-mem-layout-trans=4
- -nostandard-realloc-lhs -align array32byte -auto
- -mbranches-within-32B-boundaries -ljemalloc
- -L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using both Fortran and C:
- -w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
- -flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo
- -no-prec-div -qopt-prefetch -ffinite-math-only
- -qopt-multiple-gather-scatter-by-shuffles
- -mbranches-within-32B-boundaries -nostandard-realloc-lhs
- -align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using both C and C++:
- -w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
- -flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
- -mbranches-within-32B-boundaries -ljemalloc
- -L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using Fortran, C, and C++:
- -w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
- -flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3
- -no-prec-div -qopt-prefetch -ffinite-math-only
- -qopt-multiple-gather-scatter-by-shuffles
- -mbranches-within-32B-boundaries -nostandard-realloc-lhs
- -align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6312U, 2.40GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base = 175</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_fp_peak = Not Run</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CPU2017 License: 9019</th>
<th>Test Date: Sep-2021</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor: Cisco Systems</td>
<td>Hardware Availability: Apr-2021</td>
</tr>
<tr>
<td>Tested by: Cisco Systems</td>
<td>Software Availability: Dec-2020</td>
</tr>
</tbody>
</table>

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.8 on 2021-09-09 07:58:15-0400.
Report generated on 2021-09-29 12:25:04 by CPU2017 PDF formatter v6442.
Originally published on 2021-09-28.