Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Silver 4309Y, 2.80GHz)

SPECrate®2017_fp_base = 148
SPECrate®2017_fp_peak = Not Run

Hardware
CPU Name: Intel Xeon Silver 4309Y
Max MHz: 3600
Nominal: 2800
Enabled: 16 cores, 2 chips, 2 threads/core
Orderable: 1,2 Chips
Cache L1: 32 KB I + 48 KB D on chip per core
L2: 1.25 MB I+D on chip per core
L3: 12 MB I+D on chip per chip
Other: None
Memory: 2 TB (32 x 64 GB 2Rx4 PC4-3200V-R, running at 2666)
Storage: 1 x 240 GB M2 SSD
Other: None

Software
OS: SUSE Linux Enterprise Server 15 SP2
5.3.18-22-default
Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++
Compiler Build 20201113 for Linux;
Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux
Parallel: No
Firmware: Version 4.2.1d released Jul-2021
File System: btrfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS and OS set to prefer performance at the cost of additional power usage
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Silver 4309Y, 2.80GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
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<th>Ratio</th>
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<td>503.bwaves_r</td>
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<td>911</td>
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<td>554.roms_r</td>
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<td>67.8</td>
<td>749</td>
<td>67.9</td>
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</tr>
</tbody>
</table>

SPECrate®2017_fp_base = 148
SPECrate®2017_fp_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOC_CONF = "retain:true"

General Notes
Binaries compiled on a system with 1x Intel Core i9–7940X CPU + 64GB RAM memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Silver 4309Y, 2.80GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECrate®2017_fp_base = 148
SPECrate®2017_fp_peak = Not Run

Test Date: Aug-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

General Notes (Continued)

sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numacl i.e.:
numacl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDDC Sparing set to Disabled
Patrol Scrub set to Disabled
Enhanced CPU performance set to Auto
Processor C6 Report set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16aaca64d
running on localhost Tue Aug 24 19:28:56 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
   model name : Intel(R) Xeon(R) Silver 4309Y CPU @ 2.80GHz
     2 "physical id"s (chips)
     32 "processors"
  cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
      cpu cores : 8
      siblings : 16
      physical 0: cores 0 1 2 3 4 5 6 7
      physical 1: cores 0 1 2 3 4 5 6 7

From lscpu from util-linux 2.33.1:

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Silver 4309Y, 2.80GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base</th>
<th>148</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_fp_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

Platform Notes (Continued)

<table>
<thead>
<tr>
<th>Architecture:</th>
<th>x86_64</th>
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</thead>
<tbody>
<tr>
<td>CPU op-mode(s):</td>
<td>32-bit, 64-bit</td>
</tr>
<tr>
<td>Byte Order:</td>
<td>Little Endian</td>
</tr>
<tr>
<td>Address sizes:</td>
<td>46 bits physical, 57 bits virtual</td>
</tr>
<tr>
<td>CPU(s):</td>
<td>32</td>
</tr>
<tr>
<td>On-line CPU(s) list:</td>
<td>0-31</td>
</tr>
<tr>
<td>Thread(s) per core:</td>
<td>2</td>
</tr>
<tr>
<td>Core(s) per socket:</td>
<td>8</td>
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<tr>
<td>Socket(s):</td>
<td>2</td>
</tr>
<tr>
<td>NUMA node(s):</td>
<td>2</td>
</tr>
<tr>
<td>Vendor ID:</td>
<td>GenuineIntel</td>
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<tr>
<td>CPU family:</td>
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<tr>
<td>Model:</td>
<td>106</td>
</tr>
<tr>
<td>Model name:</td>
<td>Intel(R) Xeon(R) Silver 4309Y CPU @ 2.80GHz</td>
</tr>
<tr>
<td>Stepping:</td>
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<tr>
<td>CPU MHz:</td>
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<td>CPU max MHz:</td>
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<td>CPU min MHz:</td>
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<td>BogoMIPS:</td>
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<tr>
<td>L1i cache:</td>
<td>32K</td>
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<tr>
<td>L2 cache:</td>
<td>1280K</td>
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<tr>
<td>L3 cache:</td>
<td>12288K</td>
</tr>
<tr>
<td>NUMA node0 CPU(s):</td>
<td>0-7,16-23</td>
</tr>
<tr>
<td>NUMA node1 CPU(s):</td>
<td>8-15,24-31</td>
</tr>
<tr>
<td>Flags:</td>
<td>fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abml3nowprefetch cpuid_fault epb cat_13 invpcid_single ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnum flexpriority ept vpid ept_ad fsbgbase tsc_adjust bni hle avx2 smep bmi2 erms invpcid rtm cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha_ni avx512bw avx512vl xsaveopt xsaves xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local wbinvd dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_kgcd req avx512vmbi umip pku ospke avx512_vmbi2 gfnl vaes vpclmulqdq avx512_vnni avx512_bitalg tme avx512_vpopcntdq la57 rdrid md_clear pconfig flush_l1d arch_capabilities</td>
</tr>
</tbody>
</table>

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 2 nodes (0-1)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Silver 4309Y, 2.80GHz)

SPECrate®2017_fp_base = 148
SPECrate®2017_fp_peak = Not Run

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
<th>Test Date:</th>
<th>Aug-2021</th>
</tr>
</thead>
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<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
<td>Hardware Availability:</td>
<td>Apr-2021</td>
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<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
<td>Software Availability:</td>
<td>Dec-2020</td>
</tr>
</tbody>
</table>

Platform Notes (Continued)

node 0 cpus: 0 1 2 3 4 5 6 7 16 17 18 19 20 21 22 23
node 0 size: 1031746 MB
node 0 free: 1031085 MB
node 1 cpus: 8 9 10 11 12 13 14 15 24 25 26 27 28 29 30 31
node 1 size: 1032184 MB
node 1 free: 1031728 MB
node distances:
node 0 1
0: 10 20
1: 20 10

From /proc/meminfo
MemTotal: 2113465476 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*

uname -a:
Linux localhost 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2018-3639 (Speculative Store Bypass): Mitigation: usercopy/swapsgs barriers and __user pointer sanitization
CVE-2017-5753 (Spectre variant 1): Mitigation: Enhanced IBRS, IBPB:
CVE-2017-5715 (Spectre variant 2):
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Silver 4309Y, 2.80GHz)

Platform Notes (Continued)
conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Aug 24 14:27

SPEC is set to: /home/cpu2017

Filesystem     Type   Size  Used Avail Use% Mounted on
/dev/sda2      btrfs  222G   14G  207G   7% /home

From /sys/devices/virtual/dmi/id
Vendor:         Cisco Systems Inc
Product:        UCSC-C240-M6S
Serial:         WZP24460JDQ

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you
interpret this section. The 'dmidecode' program reads system data which is "intended to
allow hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200, configured at 2666

BIOS:
BIOS Vendor:    Cisco Systems, Inc.
BIOS Version:   C240M6.4.2.1d.0.0730210924
BIOS Date:      07/30/2021
BIOS Revision:  5.22

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C               | 519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)
==============================================================================
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================

C++             | 508.namd_r(base) 510.parest_r(base)
==============================================================================
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Silver 4309Y, 2.80GHz)

SPECraten®2017_fp_base = 148
SPECraten®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Aug-2021
Tested by: Cisco Systems
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Compiler Version Notes (Continued)

==============================================================================
C++, C          | 511.povray_r(base) 526.blender_r(base)
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved. 
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved. 

==============================================================================
C++, C, Fortran | 507.cactuBSSN_r(base)
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved. 
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on  
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved. 

==============================================================================
Fortran         | 503.bwaves_r(base) 549.fotonik3d_r(base) 554.roms_r(base)
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on  
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved. 

==============================================================================
Fortran, C      | 521.wrf_r(base) 527.cam4_r(base)
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on  
Intel(R) 64, Version 2021.1 Build 20201112_000000
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Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Silver 4309Y, 2.80GHz)

SPEC CPU®2017 Floating Point Rate Result

SPECraten™2017_fp_base = 148
SPECraten™2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icx

Benchmarks using both C and C++:
icpx icx

Benchmarks using Fortran, C, and C++:
icpx icx ifort

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX2 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-ll/usr/local/jemalloc64-5.0.1/lib

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Silver 4309Y, 2.80GHz)

SPECRate®2017_fp_base = 148
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
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Base Optimization Flags (Continued)

C++ benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX2 -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Fortran benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX2 -O3 -ipo -no-prec-div
-qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using both Fortran and C:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX2 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-nostandard-realloc-lhs -align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using both C and C++:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX2 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using Fortran, C, and C++:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX2 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-nostandard-realloc-lhs -align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml
## SPEC CPU®2017 Floating Point Rate Result

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**Cisco Systems**
Cisco UCS C240 M6 (Intel Xeon Silver 4309Y, 2.80GHz)

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**CPU2017 License:** 9019
**Test Sponsor:** Cisco Systems
**Tested by:** Cisco Systems

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.8 on 2021-08-24 19:28:55-0400.
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