**Cisco Systems**
Cisco UCS C240 M6 (Intel Xeon Silver 4309Y, 2.80GHz)

<table>
<thead>
<tr>
<th>Software</th>
<th>Hardware</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS:</td>
<td>SUSE Linux Enterprise Server 15 SP2</td>
</tr>
<tr>
<td>Compiler:</td>
<td>C/C++ Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux; Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux</td>
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<tr>
<td>Parallel:</td>
<td>Yes</td>
</tr>
<tr>
<td>File System:</td>
<td>btrfs</td>
</tr>
<tr>
<td>System State:</td>
<td>Run level 3 (multi-user)</td>
</tr>
<tr>
<td>Base Pointers:</td>
<td>64-bit</td>
</tr>
<tr>
<td>Peak Pointers:</td>
<td>Not Applicable</td>
</tr>
<tr>
<td>Other:</td>
<td>jemalloc memory allocator V5.0.1</td>
</tr>
<tr>
<td>Power Management:</td>
<td>BIOS and OS set to prefer performance at the cost of additional power usage</td>
</tr>
</tbody>
</table>

| CPU2017 License: | 9019                                           |
| Test Sponsor:    | Cisco Systems                                  |
| Tested by:       | Cisco Systems                                  |
| Test Date:       | Aug-2021                                       |
| Hardware Availability: | Apr-2021                                      |
| Software Availability: | Dec-2020                                     |

---

**SPEC CPU®2017 Integer Speed Result**

### CPU Name: Intel Xeon Silver 4309Y
- Max MHz: 3600
- Nominal: 2800
- Enabled: 16 cores, 2 chips
- Orderable: 1.2 Chips
- Cache L1: 32 KB I+48 KB D on chip per core
- L2: 1.25 MB I+D on chip per core
- L3: 12 MB I+D on chip per chip
- Other: None
- Memory: 2 TB (32 x 64 GB 2Rx4 PC4-3200V-R, running at 2666)
- Storage: 1 x 240 GB M2 SSD
- Other: None

<table>
<thead>
<tr>
<th>Threads</th>
<th>SPECspeed®2017_int_base = 11.0</th>
<th>SPECspeed®2017_int_peak = Not Run</th>
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<tbody>
<tr>
<td>600.perbench_s</td>
<td>7.94</td>
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<tr>
<td>602.gcc_s</td>
<td>10.1</td>
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<tr>
<td>605.mcf_s</td>
<td>19.5</td>
<td></td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>6.89</td>
<td></td>
</tr>
<tr>
<td>623.xalancbmk_s</td>
<td>13.6</td>
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</tr>
<tr>
<td>625.x264_s</td>
<td>16.7</td>
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<tr>
<td>631.deepsjeng_s</td>
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<tr>
<td>641.leela_s</td>
<td>5.03</td>
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<tr>
<td>648.exchange2_s</td>
<td>19.9</td>
<td></td>
</tr>
<tr>
<td>657.xz_s</td>
<td>15.5</td>
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SPEC CPU®2017 Integer Speed Result

Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Silver 4309Y, 2.80GHz)

SPECspeed®2017_int_base = 11.0
SPECspeed®2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Aug-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Base</th>
<th>Peak</th>
<th>Base</th>
<th>Peak</th>
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<tr>
<td></td>
<td>Seconds</td>
<td>Seconds</td>
<td>Seconds</td>
<td>Ratio</td>
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<td>620.omnetpp_s</td>
<td>16</td>
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<tr>
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<td>104</td>
<td>13.6</td>
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<tr>
<td>625.x264_s</td>
<td>16</td>
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<td>641.leela_s</td>
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<td>648.exchange2_s</td>
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<td>19.9</td>
<td>148</td>
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<tr>
<td>657.xz_s</td>
<td>16</td>
<td>317</td>
<td>317</td>
<td>19.5</td>
<td>318</td>
</tr>
</tbody>
</table>

SPECspeed®2017_int_base = 11.0
SPECspeed®2017_int_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,scatter"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOC_CONF = "retain:true"
OMP_STACKSIZE = "192M"

General Notes
Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
 sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Silver 4309Y, 2.80GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

General Notes (Continued)

numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel Hyper-Threading Technology set to Disabled
DCU Streamer Prefetch set to Disabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDDC Sparing set to Disabled
Patrol Scrub set to Disabled
Enhanced CPU performance set to Auto
Processor C6 Report set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acfc64d

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4309Y CPU @ 2.80GHz
  2 "physical id"s (chips)
  16 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 8
  siblings : 8
  physical 0: cores 0 1 2 3 4 5 6 7
  physical 1: cores 0 1 2 3 4 5 6 7

From lscpu from util-linux 2.33.1:
  Architecture: x86_64
  CPU op-mode(s): 32-bit, 64-bit

(Continued on next page)
### Platform Notes (Continued)

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Byte Order</td>
<td>Little Endian</td>
</tr>
<tr>
<td>Address sizes</td>
<td>46 bits physical, 57 bits virtual</td>
</tr>
<tr>
<td>CPU(s)</td>
<td>16</td>
</tr>
<tr>
<td>On-line CPU(s) list</td>
<td>0-15</td>
</tr>
<tr>
<td>Thread(s) per core</td>
<td>1</td>
</tr>
<tr>
<td>Core(s) per socket</td>
<td>8</td>
</tr>
<tr>
<td>Socket(s)</td>
<td>2</td>
</tr>
<tr>
<td>NUMA node(s)</td>
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</tr>
<tr>
<td>Vendor ID</td>
<td>GenuineIntel</td>
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<tr>
<td>CPU family</td>
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</tr>
<tr>
<td>Model</td>
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<tr>
<td>Model name</td>
<td>Intel(R) Xeon(R) Silver 4309Y CPU @ 2.80GHz</td>
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<tr>
<td>Stepping</td>
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</tr>
<tr>
<td>CPU MHz</td>
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<tr>
<td>CPU min MHz</td>
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<td>Virtualization</td>
<td>VT-x</td>
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<tr>
<td>L1d cache</td>
<td>48K</td>
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<tr>
<td>L1i cache</td>
<td>32K</td>
</tr>
<tr>
<td>L2 cache</td>
<td>1280K</td>
</tr>
<tr>
<td>L3 cache</td>
<td>12288K</td>
</tr>
<tr>
<td>NUMA node0 CPU(s)</td>
<td>0-7</td>
</tr>
<tr>
<td>NUMA node1 CPU(s)</td>
<td>8-15</td>
</tr>
<tr>
<td>Flags</td>
<td>fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 lse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3nowprefetch cpuid_fault epb cat_l3 invpcid_single ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi flexpriority ept vpid ept_ad fsgsbase tsc_adjust bds bdle avx2 smep bmi2 erms invpcid rtm cmq rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha ni avx512bw avx512vl xsaveopt xsavec xaxvib1 xsaves cmq_llc cmq_occuc_llc cmq_mbb_total cmq_mbb_local wbinvd dtiwarm ida arat pln plts hwp hwp_act_window hwp_epp hwp_pkgreq avx512vmbi umip pku ospe avx512vvmi2 gfini vaes vpcmklseq dq avx512_vnni avx512_bitalg tme avx512_vpopcntdq 1a57 rdpid md_clear pconfig flush_lid arch_capabilities</td>
</tr>
</tbody>
</table>

```
 From numactl --hardware
 WARNING: a numactl 'node' might or might not correspond to a physical chip.
 available: 2 nodes (0-1)
 node 0 cpus: 0 1 2 3 4 5 6 7
 node 0 size: 1031782 MB
```

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Silver 4309Y, 2.80GHz)

SPEC CPU®2017 Integer Speed Result
Copyright 2017-2021 Standard Performance Evaluation Corporation

Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Silver 4309Y, 2.80GHz)

SPECspeed®2017_int_base = 11.0
SPECspeed®2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Aug-2021
Tested by: Cisco Systems
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Platform Notes (Continued)

node 0 free: 1031345 MB
node 1 cpus: 8 9 10 11 12 13 14 15
node 1 size: 1032152 MB
node 1 free: 1031597 MB
node distances:
  node 0 1
  0: 10 20
  1: 20 10

From /proc/meminfo
MemTotal:       2113469064 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15-SP2"
    VERSION_ID="15.2"
    PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
Linux localhost 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit):
CVE-2018-3620 (L1 Terminal Fault):
Microarchitectural Data Sampling:
CVE-2017-5754 (Meltdown):
CVE-2018-3639 (Speculative Store Bypass):
CVE-2017-5753 (Spectre variant 1):
CVE-2017-5715 (Spectre variant 2):
CVE-2020-0543 (Special Register Buffer Data Sampling):

Not affected
Not affected
Not affected
Mitigation: Speculative Store Bypass disabled via prctl and seccomp
Mitigation: usercopy/swapgs barriers and __user pointer sanitization
Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
Not affected

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Silver 4309Y, 2.80GHz)

SPECspeed®2017_int_base = 11.0
SPECspeed®2017_int_peak = Not Run

CPU2017 License: 9019
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Platform Notes (Continued)

CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Aug 25 20:32

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda2 btrfs 222G 18G 203G 9% /home

From /sys/devices/virtual/dmi/id
Vendor: Cisco Systems Inc
Product: UCSC-C240-M6S
Serial: WZP24460JDQ

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
  32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200, configured at 2666

BIOS:
  BIOS Vendor: Cisco Systems, Inc.
  BIOS Version: C240M6.4.2.1d.0.0730210924
  BIOS Date: 07/30/2021
  BIOS Revision: 5.22

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C       | 600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base)
        | 625.x264_s(base) 657.xz_s(base)
==============================================================================
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================
C++     | 620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base)
        | 641.leela_s(base)
==============================================================================
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
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(Continued on next page)
## Cisco Systems

Cisco UCS C240 M6 (Intel Xeon Silver 4309Y, 2.80GHz)

<table>
<thead>
<tr>
<th>SPECspeed®2017_int_base</th>
<th>11.0</th>
</tr>
</thead>
</table>

| SPECspeed®2017_int_peak | Not Run |

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
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<tbody>
<tr>
<td>Test Sponsor:</td>
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<tr>
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</tr>
</tbody>
</table>

### Compiler Version Notes (Continued)

Fortran | 648.exchange2_s(base)

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000

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### Base Compiler Invocation

C benchmarks:
- icx

C++ benchmarks:
- icpx

Fortran benchmarks:
- ifort

### Base Portability Flags

- 600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
- 602.gcc_s: -DSPEC_LP64
- 605.mcf_s: -DSPEC_LP64
- 620.omnetpp_s: -DSPEC_LP64
- 623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
- 625.x264_s: -DSPEC_LP64
- 631.deepsjeng_s: -DSPEC_LP64
- 641.leela_s: -DSPEC_LP64
- 648.exchange2_s: -DSPEC_LP64
- 657.xz_s: -DSPEC_LP64

### Base Optimization Flags

C benchmarks:
- -DSPEC_OPENMP -std=c11 -m64 -fiopenmp -Wl,-z,muldefs -xCORE-AVX512
- -O3 -ffast-math -flto -mfpmath=sse -funroll-loops
- -qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
- -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

(Continued on next page)
## SPEC CPU®2017 Integer Speed Result

**Cisco Systems**

Cisco UCS C240 M6 (Intel Xeon Silver 4309Y, 2.80GHz)

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</tbody>
</table>

### Base Optimization Flags (Continued)

**C++ benchmarks:**
- DSPEC_OPENMP
- -m64
- -Wl,-z,muldefs
- -xCORE-AVX512
- -O3
- -ffast-math
- -flto
- -mfpmath=sse
- -funroll-loops
- -qopt-mem-layout-trans=4
- -mbranches-within-32B-boundaries
- -L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin/
- -lqkmalloc

**Fortran benchmarks:**
- -m64
- -xCORE-AVX512
- -O3
- -ipo
- -no-prec-div
- -qopt-mem-layout-trans=4
- -nostandard-realloc-lhs
- -align array32byte
- -auto
- -mbranches-within-32B-boundaries

The flags files that were used to format this result can be browsed at:

You can also download the XML flags sources by saving the following links: