**Cisco Systems**  
Cisco UCS C220 M6 (Intel Xeon Gold 6334, 3.60GHz)  

<table>
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<tr>
<th>Threads</th>
<th>SPECspeed®2017_int_base = 11.6</th>
<th>SPECspeed®2017_int_peak = 11.9</th>
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<tr>
<td>600.perlbench_s 16</td>
<td>7.46</td>
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<tr>
<td>602.gcc_s 16</td>
<td>10.9</td>
<td>11.3</td>
</tr>
<tr>
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<td>8.52</td>
<td>20.2</td>
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<td>620.omnetpp_s 16</td>
<td>14.0</td>
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<tr>
<td>623.xalancbmk_s 16</td>
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<td>631.deepsjeng_s 16</td>
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<tr>
<td>641.leela_s 16</td>
<td></td>
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<tr>
<td>648.exchange2_s 16</td>
<td></td>
<td></td>
</tr>
<tr>
<td>657.xz_s 16</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Hardware**

- **CPU Name:** Intel Xeon Gold 6334  
- **Max MHz:** 3700  
- **Nominal:** 3600  
- **Enabled:** 16 cores, 2 chips  
- **Orderable:** 1.2 Chips  
- **Cache L1:** 32 KB I + 48 KB D on chip per core  
- **L2:** 1.25 MB I+D on chip per core  
- **L3:** 18 MB I+D on chip per core  
- **Other:** None  
- **Memory:** 1 TB (32 x 32 GB 2Rx4 PC4-3200V-R)  
- **Storage:** 1 x 240 GB SATA SSD  
- **Other:** None

**Software**

- **OS:** SUSE Linux Enterprise Server 15 SP2 5.3.18-22-default  
- **Compiler:** C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux; Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux; C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux  
- **Parallel:** Yes  
- **Firmware:** Version 4.2.1d released Jul-2021  
- **File System:** btrfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** 64-bit  
- **Other:** jemalloc memory allocator V5.0.1  
- **Power Management:** BIOS and OS set to prefer performance at the cost of additional power usage
Cisco Systems

Cisco UCS C220 M6 (Intel Xeon Gold 6334, 3.60GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECspeed®2017_int_base = 11.6
SPECspeed®2017_int_peak = 11.9

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<td>301</td>
<td>20.5</td>
<td><strong>301</strong></td>
<td><strong>20.5</strong></td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:
- KMP_AFFINITY = "granularity=fine,scatter"
- LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
- MALLOC_CONF = "retain:true"
- OMP_STACKSIZE = "192M"

### General Notes

Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM memory using Redhat Enterprise Linux 8.0

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3> /proc/sys/vm/drop_caches
```

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6334, 3.60GHz)

SPECspeed®2017_int_base = 11.6
SPECspeed®2017_int_peak = 11.9

CPU2017 License: 9019
Test Date: Aug-2021
Test Sponsor: Cisco Systems
Hardware Availability: Jun-2021
Tested by: Cisco Systems
Software Availability: Dec-2020

General Notes (Continued)

Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
UPI Link Enablement set to 1
UPI Power Management set to Enabled
Sub NUMA Clustering set to Disabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDDC Sparing set to Disabled
Patrol Scrub set to Disabled
Enhanced CPU performance set to Auto
Energy Efficient Turbo set to Enabled
Processor C6 Report set to Enabled
Processor C1E set to Enabled
Intel Hyper-Threading Technology set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891e0e16acafc64d
running on localhost Tue Aug 24 20:48:55 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6334 CPU @ 3.60GHz
  2 "physical id"s (chips)
  16 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 8
siblings : 8
physical 0: cores 0 1 2 3 4 5 6 7
physical 1: cores 0 1 2 3 4 5 6 7

From lscpu from util-linux 2.33.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 16
On-line CPU(s) list: 0-15

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6334, 3.60GHz)

SPECspeak®2017_int_base = 11.6
SPECspeed®2017_int_peak = 11.9

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Aug-2021
Tested by: Cisco Systems
Hardware Availability: Jun-2021
Software Availability: Dec-2020

Platform Notes (Continued)

Thread(s) per core: 1
Core(s) per socket: 8
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Gold 6334 CPU @ 3.60GHz
Stepping: 6
CPU MHz: 2861.316
CPU max MHz: 3700.0000
CPU min MHz: 800.0000
BogoMIPS: 7200.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 18432K
NUMA node0 CPU(s): 0-7
NUMA node1 CPU(s): 8-15
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xptr pdcm pclid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invvpidd_single ssbd
mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vmmx flexpriority ept vpid ept_ad
fsxgamma tsc_adjust bmi1 hle avx2 smep bmi2 ets invpcid_single ssbd
mqa ibrs ibpb stibp ibrs_enhanced tpr_shadow vmmx flexpriority ept vpid ept_ad
fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm rdt_a avx512f
avx512dqd rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha ni
avx512bw avx512vl xsaves opt xsaveopt xsaves xsavec xsavec xsave xsaves cqm_llc cqm_occu
llc cqm_mbttotal cqm_mbb_local wbnoinvd dtherm ida arat pln pts hwp hwp_actwindow hwp_epp
hwp_pkg_rex avx512vbi umip pku ospke avx512_vbmi2 gfni vaes vpclmulqdq avx512_vnni
avx512_bitalg tme avx512_vpopcntdq 1a57 rdpid md_clear pconfig flush_lld
arch_capabilities

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7
node 0 size: 515652 MB
node 0 free: 515078 MB
node 1 cpus: 8 9 10 11 12 13 14 15
node 1 size: 516090 MB
node 1 free: 515695 MB

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6334, 3.60GHz)

SPECspeed®2017_int_base = 11.6
SPECspeed®2017_int_peak = 11.9

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

node distances:
node  0  1
0:  10  20
1:  20  10

From /proc/meminfo
MemTotal:       1056505692 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release*/etc/*version*
os-release:
NAME="SLES"
VERSION="15-SP2"
VERSION_ID="15.2"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
Linux localhost 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Mitigation: Speculative Store
CVE-2018-3639 (Speculative Store Bypass): Bypass disabled via prctl and
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs
CVE-2017-5715 (Spectre variant 2): barriers and __user pointer
CVE-2020-0543 (Special Register Buffer Data Sampling): sanitization
CVE-2019-11135 (TSX Asynchronous Abort): Mitigation: Enhanced IBRS, IBPB:
conditional, RSB filling

run-level 3 Aug 24 20:41

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6334, 3.60GHz)

SPECspeed®2017_int_base = 11.6
SPECspeed®2017_int_peak = 11.9

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)
SPEC is set to: /home/cpu2017
Filesystem     Type   Size  Used Avail Use% Mounted on
/dev/sda2      btrfs  222G   35G  186G  16% /home

From /sys/devices/virtual/dmi/id
Vendor: Cisco Systems Inc
Product: UCSC-C220-M6S
Serial: WZP24430ADF

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
32x 0xCE00 M393A4K40DB3-CWE 32 GB 2 rank 3200

BIOS:
BIOS Vendor: Cisco Systems, Inc.
BIOS Version: C220M6.4.2.1d.0.0730210924
BIOS Date: 07/30/2021
BIOS Revision: 5.22

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C       | 600.perlbench_s(peak)
==============================================================================
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================
C       | 600.perlbench_s(base) 602.gcc_s(base, peak) 605.mcf_s(base, peak)
| 625.x264_s(base, peak) 657.xz_s(base, peak)
==============================================================================
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================
C       | 600.perlbench_s(peak)
(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6334, 3.60GHz)

SPEC®2017_int_base = 11.6
SPEC®2017_int_peak = 11.9

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Aug-2021
Hardware Availability: Jun-2021
Software Availability: Dec-2020

Compiler Version Notes (Continued)

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================
C       | 600.perlbench_s(base) 602.gcc_s(base, peak) 605.mcf_s(base, peak)
| 625.x264_s(base, peak) 657.xz_s(base, peak)
==============================================================================
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================
C++     | 620.omnetpp_s(base, peak) 623.xalancbmk_s(base, peak)
| 631.deepsjeng_s(base, peak) 641.leela_s(base, peak)
==============================================================================
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================
Fortran | 648.exchange2_s(base, peak)
==============================================================================
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort
## Cisco Systems

Cisco UCS C220 M6 (Intel Xeon Gold 6334, 3.60GHz)

<table>
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<th>SPECspeed®2017_int_base = 11.6</th>
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<td>Hardware Availability: Jun-2021</td>
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<th>CPU2017 License: 9019</th>
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<tbody>
<tr>
<td>Test Sponsor: Cisco Systems</td>
<td>Software Availability: Dec-2020</td>
</tr>
</tbody>
</table>

### Base Portability Flags

- 600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
- 602.gcc_s: -DSPEC_LP64
- 605.mcf_s: -DSPEC_LP64
- 620.omnetpp_s: -DSPEC_LP64
- 623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
- 625.x264_s: -DSPEC_LP64
- 631.deepsjeng_s: -DSPEC_LP64
- 641.leela_s: -DSPEC_LP64
- 648.exchange2_s: -DSPEC_LP64
- 657.xz_s: -DSPEC_LP64

### Base Optimization Flags

**C benchmarks:**
- -DSPEC_OPENMP -std=c11 -m64 -fopenmp -Wl,-z,muldefs -xCORE-AVX512
- -03 -ffast-math -flto -mfpmath=sse -funroll-loops
- -qopt-mem-layout-trans=4 -mbranches-within-32B-boundsaries
- -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

**C++ benchmarks:**
- -DSPEC_OPENMP -m64 -Wl,-z,muldefs -xCORE-AVX512 -03 -ffast-math
- -flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
- -mbranches-within-32B-boundsaries
- -L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin/
  -lqkmalloc

**Fortran benchmarks:**
- -m64 -xcORE-AVX512 -03 -ipo -no-prec-div -qopt-mem-layout-trans=4
- -nostandard-realloc-lhs -align array32byte -auto
- -mbranches-within-32B-boundsaries

### Peak Compiler Invocation

**C benchmarks (except as noted below):**
- icx
- 600.perlbench_s: icc

**C++ benchmarks:**
- icpx

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6334, 3.60GHz)

SPECsrate®2017_int_base = 11.6
SPECsrate®2017_int_peak = 11.9

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2021
Hardware Availability: Jun-2021
Software Availability: Dec-2020

Peak Compiler Invocation (Continued)
Fortran benchmarks:
ifort

Peak Portability Flags
Same as Base Portability Flags

Peak Optimization Flags
C benchmarks:

600.perlbench_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)
-xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-strict-overflow
-mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

602.gcc_s: -m64 -std=c11 -Wl,-z,muldefs -fprofile-generate(pass 1)
-fprofile-use=default.profdata(pass 2) -xCORE-AVX512 -flto
-Ofast(pass 1) -O3 -ffast-math -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

605.mcf_s: basepeak = yes

625.x264_s: -DSPEC_OPENMP -fiopenmp -std=c11 -m64 -Wl,-z,muldefs
-xCORE-AVX512 -flto -O3 -ffast-math
-qopt-mem-layout-trans=4 -fno-alias
-mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

657.xz_s: basepeak = yes

C++ benchmarks:

620.omnetpp_s: basepeak = yes

623.xalancbmk_s: basepeak = yes

631.deepsjeng_s: basepeak = yes

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6334, 3.60GHz)

| SPECspeed®2017_int_base = 11.6 |
| SPECspeed®2017_int_peak = 11.9 |

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Aug-2021
Hardware Availability: Jun-2021
Software Availability: Dec-2020

**Peak Optimization Flags (Continued)**

641.leela_s: basepeak = yes

Fortran benchmarks:
648.exchange2_s: basepeak = yes

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml