# SPEC CPU®2017 Integer Rate Result

**Cisco Systems**

Cisco UCS C220 M6 (Intel Xeon Silver 4309Y, 2.80GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base = 133</th>
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<tbody>
<tr>
<td>SPECrate®2017_int_peak = 137</td>
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**CPU2017 License:** 9019  
**Test Sponsors:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Aug-2021  
**Hardware Availability:** Jun-2021  
**Software Availability:** Dec-2020

## Hardware

- **CPU Name:** Intel Xeon Silver 4309Y  
- **Max MHz:** 3600  
- **Nominal:** 2800  
- **Enabled:** 16 cores, 2 chips, 2 threads/core  
- **Orderable:** 1.2 Chips  
- **Cache L1:** 32 KB I + 48 KB D on chip per core  
- **L2:** 1.25 MB I+D on chip per core  
- **L3:** 12 MB I+D on chip per chip  
- **Other:** None  
- **Memory:** 1 TB (32 x 32 GB 2Rx4 PC4-3200V-R, running at 2666)  
- **Storage:** 1 x 240 GB SATA SSD  
- **Other:** None

## Software

- **OS:** SUSE Linux Enterprise Server 15 SP2  
  5.3.18-22-default  
- **Compiler:**  
  C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux;  
  Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux;  
  C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux  
- **Parallel:** No  
- **Firmware:** Version 4.2.1d released Jul-2021  
- **File System:** btrfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** 32/64-bit  
- **Other:** jemalloc memory allocator V5.0.1  
- **Power Management:** BIOS and OS set to prefer performance at the cost of additional power usage

## Copies

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</tr>
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spec

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<th>Seconds</th>
<th>Ratio</th>
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<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
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<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
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<tr>
<td>500.perlbench_r</td>
<td>32</td>
<td>573</td>
<td>89.0</td>
<td>573</td>
<td>89.9</td>
<td>572</td>
<td>89.0</td>
<td>32</td>
<td>491</td>
<td>104</td>
<td>491</td>
<td>104</td>
<td>490</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>32</td>
<td>406</td>
<td>112</td>
<td>413</td>
<td>110</td>
<td>408</td>
<td>111</td>
<td>32</td>
<td>361</td>
<td>126</td>
<td>363</td>
<td>125</td>
<td>360</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>32</td>
<td>225</td>
<td>229</td>
<td>227</td>
<td>228</td>
<td>228</td>
<td>227</td>
<td>32</td>
<td>225</td>
<td>229</td>
<td>227</td>
<td>228</td>
<td>222</td>
</tr>
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<td>32</td>
<td>510</td>
<td>82.3</td>
<td>508</td>
<td>82.7</td>
<td>507</td>
<td>82.8</td>
<td>32</td>
<td>510</td>
<td>82.3</td>
<td>508</td>
<td>82.7</td>
<td>507</td>
</tr>
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<td>523.xalancbmk_r</td>
<td>32</td>
<td>201</td>
<td>168</td>
<td>200</td>
<td>169</td>
<td>200</td>
<td>169</td>
<td>32</td>
<td>201</td>
<td>168</td>
<td>200</td>
<td>169</td>
<td>200</td>
</tr>
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<td>32</td>
<td>207</td>
<td>271</td>
<td>207</td>
<td>271</td>
<td>207</td>
<td>271</td>
<td>32</td>
<td>198</td>
<td>284</td>
<td>198</td>
<td>283</td>
<td>198</td>
</tr>
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<td>32</td>
<td>360</td>
<td>102</td>
<td>361</td>
<td>102</td>
<td>360</td>
<td>102</td>
<td>32</td>
<td>360</td>
<td>102</td>
<td>361</td>
<td>102</td>
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<td>534</td>
<td>99.2</td>
<td>534</td>
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<td>534</td>
<td>99.3</td>
<td>32</td>
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<td>276</td>
<td>303</td>
<td>277</td>
<td>303</td>
<td>277</td>
<td>32</td>
<td>304</td>
<td>276</td>
<td>303</td>
<td>277</td>
<td>303</td>
</tr>
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<td>32</td>
<td>484</td>
<td>71.3</td>
<td>484</td>
<td>71.4</td>
<td>485</td>
<td>71.2</td>
<td>32</td>
<td>494</td>
<td>70.0</td>
<td>495</td>
<td>69.8</td>
<td>494</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = 
"/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"
MALLOCONF = "retain:true"

General Notes
Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM
memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:

(Continued on next page)
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SPECrate®2017_int_base = 133
SPECrate®2017_int_peak = 137

General Notes (Continued)

numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
UPI Link Enablement set to 1
UPI Power Management set to Enabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDDC Sparing set to Disabled
Patrol Scrub set to Disabled
Energy Efficient Turbo set to Enabled
Processor C6 Report set to Enabled
Processor C1E set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acfc64d
running on localhost Sat Aug 28 07:48:03 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4309Y CPU @ 2.80GHz
  2 "physical id"s (chips)
  32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 8
siblings : 16
  physical 0: cores 0 1 2 3 4 5 6 7
  physical 1: cores 0 1 2 3 4 5 6 7

(Continued on next page)
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
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Platform Notes (Continued)

From lscpu from util-linux 2.33.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 32
On-line CPU(s) list: 0-31
Thread(s) per core: 2
Core(s) per socket: 8
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Silver 4309Y CPU @ 2.80GHz
Stepping: 6
CPU MHz: 908.120
CPU max MHz: 3600.0000
CPU min MHz: 800.0000
BogoMIPS: 5600.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 12288K
NUMA node0 CPU(s): 0-7, 16-23
NUMA node1 CPU(s): 8-15, 24-31
Flags: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtrr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 invpcid_single ssbd mba ibrs ibbp ibrs_enhanced tpr_shadow vnmi flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erts invpcid rtm cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha_ni avx512bw avx512vl xsaveopt xsaveprec xsaves xsavec xsaveopt avx12c xmaskmov avx12f128 xsaveopt avx512f128 smm cmipisten cmipimc persisted cmipismt cmipisst dtes64_64bit_avx2 smmila stibp tpr_shadow tpr迢ehift tpr-disable flushbytew flushdtb avx512cfp f16c xsaveopt k ausync epccmp Fnma epcompte qdic qmpcoto armv8a-crcfn fma mcm这部少 tpm pafi tpm_u512k bitrange tpr_shadow tpr_tisa mish

/proc/cpuinfo cache data
  cache size : 12288 KB

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.

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**Platform Notes (Continued)**

available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 16 17 18 19 20 21 22 23
node 0 size: 515651 MB
node 0 free: 515057 MB
node 1 cpus: 8 9 10 11 12 13 14 15 24 25 26 27 28 29 30 31
node 1 size: 516089 MB
node 1 free: 515580 MB
node distances:
node 0 1
  0: 10  20
  1: 20  10

From /proc/meminfo
MemTotal: 1056502100 kB
HugePages_Total: 0
Hugepagesize: 2048 kB
/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15-SP2"
    VERSION_ID="15.2"
    PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
Linux localhost 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swaps barriers and __user pointer sanitization

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Platform Notes (Continued)

CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected
run-level 3 Aug 28 07:41
SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sdb2 btrfs 222G 33G 189G 15% /home

From /sys/devices/virtual/dmi/id
Vendor: Cisco Systems Inc
Product: UCSC-C220-M6S
Serial: WZP244104TF

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
  32x 0xCE00 M393A4K40DB3-CWE 32 GB 2 rank 3200, configured at 2666

BIOS:
  BIOS Vendor: Cisco Systems, Inc.
  BIOS Version: C220M6.4.2.1d.0.0730210924
  BIOS Date: 07/30/2021
  BIOS Revision: 5.22

(End of data from sysinfo program)

Compiler Version Notes

C       | 500.perlbench_r(peak) 557.xz_r(peak)
---------------------

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
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C       | 502.gcc_r(peak)
---------------------

Intel(R) oneAPI DPC+/C++ Compiler for applications running on IA-32, Version 2021.1 Build 20201113

(Continued on next page)
## Compiler Version Notes (Continued)

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C++     | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base, peak) 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
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Fortran  | 548.exchange2_r(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
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Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort
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### Base Optimization Flags

**C benchmarks:**

```
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc
```

**C++ benchmarks:**

```
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc
```

**Fortran benchmarks:**

```
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-auto -mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc
```

### Peak Compiler Invocation

**C benchmarks (except as noted below):**

```
icx
```

```
500.perlbench_r: icx
```

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Silver 4309Y, 2.80GHz)    SPECrate®2017_int_base = 133
SPECrate®2017_int_peak = 137

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>Test Sponsor:</th>
<th>Spec CPU®2017 Integer Rate Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>9019</td>
<td>Cisco Systems</td>
<td></td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
<td></td>
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</tbody>
</table>

Test Date: Aug-2021

Hardware Availability: Jun-2021

Software Availability: Dec-2020

Peak Compiler Invocation (Continued)

557.xz_r: icc

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64 -DSPEC_LINUX
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:

500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)
-xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-strict-overflow
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

502.gcc_r: -m32
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/ia32_lin
-std=gnu89 -Wl,-z,muldefs -fprofile-generate(pass 1)
-fprofile-use=default.profdata(pass 2) -xCORE-AVX512 -fto
-Ofast(pass 1) -O3 -ffast-math -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/usr/local/jemalloc32-5.0.1/lib -ljemalloc

505.mcf_r: basepeak = yes

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Silver 4309Y, 2.80GHz)

SPECrate®2017_int_base = 133
SPECrate®2017_int_peak = 137

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Aug-2021
Hardware Availability: Jun-2021
Test Sponsor: Cisco Systems
Software Availability: Dec-2020

Peak Optimization Flags (Continued)

525.x264_r: -w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -flto
-O3 -ffast-math -qopt-mem-layout-trans=4 -fno-alias
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-1qkmalloc

557.xz_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-1qkmalloc

C++ benchmarks:
520.omnetpp_r: basepeak = yes
523.xalancbmk_r: basepeak = yes
531.deepsjeng_r: basepeak = yes
541.leela_r: basepeak = yes

Fortran benchmarks:
548.exchange2_r: basepeak = yes

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml

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