Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Silver 4316, 2.30GHz)

CPU2017 License: 9019
Test Date: Aug-2021
Test Sponsor: Cisco Systems
Hardware Availability: Jun-2021
Tested by: Cisco Systems
Software Availability: Dec-2020

Software
OS: SUSE Linux Enterprise Server 15 SP2 5.3.18-22-default
Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux; Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux;
C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux
Parallel: Yes
Firmware: Version 4.2.1d released Jul-2021
File System: btrfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS and OS set to prefer performance at the cost of additional power usage

Hardware
CPU Name: Intel Xeon Silver 4316
Max MHz: 3400
Nominal: 2300
Enabled: 40 cores, 2 chips
Orderable: 1,2 Chips
Cache L1: 32 KB I + 48 KB D on chip per core
L2: 1.25 MB I+D on chip per core
L3: 30 MB I+D on chip per chip
Other: None
Memory: 1 TB (32 x 32 GB 2Rx4 PC4-3200V-R, running at 2666)
Storage: 1 x 240 GB SATA SSD
Other: None

<table>
<thead>
<tr>
<th>Test</th>
<th>SPECspeed®2017_fp_base</th>
<th>SPECspeed®2017_fp_peak</th>
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<tbody>
<tr>
<td>603.bwaves_s</td>
<td>155</td>
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</tr>
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Threads

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## Results Table

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<td><strong>108</strong></td>
<td><strong>145</strong></td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:

- KMP_AFFINITY = "granularity=fine,compact"
- LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
- MALLOC_CONF = "retain:true"
- OMP_STACKSIZE = "192M"

### General Notes

Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM
Memory using Redhat Enterprise Linux 8.0
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3 > /proc/sys/vm/drop_caches

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

(Continued on next page)
Cisco Systems
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SPECspeed®2017_fp_base = 155
SPECspeed®2017_fp_peak = 165

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2021
Hardware Availability: Jun-2021
Software Availability: Dec-2020

General Notes (Continued)


Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
UPI Link Enablement set to 1
UPI Power Management set to Enabled
Sub NUMA Clustering set to Disabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDDC Sparing set to Disabled
Patrol Scrub set to Disabled
Enhanced CPU performance set to Auto
Energy Efficient Turbo set to Enabled
Processor C6 Report set to Enabled
Processor C1E set to Enabled
Intel Hyper-Threading Technology set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acaf64d
running on localhost Tue Aug 24 22:02:17 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4316 CPU @ 2.30GHz
  2 "physical id"s (chips)
  40 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
certs from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 20
siblings : 20
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19

From lscpu from util-linux 2.33.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 40
On-line CPU(s) list: 0-39

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Silver 4316, 2.30GHz)

SPEC CPU®2017 Floating Point Speed Result
Copyright 2017-2021 Standard Performance Evaluation Corporation

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Thread(s) per core: 1
Core(s) per socket: 20
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Silver 4316 CPU @ 2.30GHz
Stepping: 6
CPU MHz: 2870.133
CPU max MHz: 3400.0000
CPU min MHz: 800.0000
BogoMIPS: 4600.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 30720K
NUMA node0 CPU(s): 0-19
NUMA node1 CPU(s): 20-39

Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invpcid_single ssbd mba ibrs ibpb ibrs_enhanced tpr_shadow vmlinux flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha ni avx512bw avx512vl xsaveopt xsaveas xsavec xsaves cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local wbnoinvd dtherm ida arat pfn pts hwp hwp_act_window hwp_epp hwp_pkg_req avx512vbmi umip pku ospke avx512_vbmi2 gfni vaes vpcmwlqdq avx512_vnni avx512_bitalg tme avx512_vpopcntdq la57 rdpid md_clear pconfig flush_l1d arch_capabilities

/platforms/cpuinfo/cache/data

CACHE size: 30720 KB

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
node 0 size: 515650 MB
node 0 free: 511575 MB
node 1 cpus: 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39
node 1 size: 516087 MB
node 1 free: 511837 MB

(Continued on next page)
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Platform Notes (Continued)

node distances:
node  0  1
  0:  10  20
  1:  20  10

From /proc/meminfo
  MemTotal:       1056499796 kB
  HugePages_Total:       0
  Hugepagesize:       2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has
performance

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15-SP2"
    VERSION_ID="15.2"
    PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
  Linux localhost 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
  x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Mitigation: Speculative Store
CVE-2018-3639 (Speculative Store Bypass): Bypass disabled via prctl and
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swaps
CVE-2017-5715 (Spectre variant 2): barriers and __user pointer
CVE-2020-0543 (Special Register Buffer Data Sampling): sanitization
CVE-2019-11135 (TSX Asynchronous Abort): Mitigation: Enhanced IBRS, IBPB:
runtime 3 Aug 24 17:42
conditional, RSB filling

(Continued on next page)
Cisco Systems
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SPECspeed®2017_fp_base = 155
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Platform Notes (Continued)

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sdb2 btrfs 222G 39G 183G 18% /home

From /sys/devices/virtual/dmi/id
Vendor: Cisco Systems Inc
Product: UCSC-C220-M6S
Serial: WZP244104TF

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
32x 0xCE00 M393A4K40DB3-CWE 32 GB 2 rank 3200, configured at 2666

BIOS:
BIOS Vendor: Cisco Systems, Inc.
BIOS Version: C220M6.4.2.1d.0.0730210924
BIOS Date: 07/30/2021
BIOS Revision: 5.22

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C | 619.lbm_s(base, peak) 638.imagick_s(base, peak)
  644.nab_s(base)
==============================================================================
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================

==============================================================================
C | 644.nab_s(peak)
==============================================================================
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================

==============================================================================
C | 619.lbm_s(base, peak) 638.imagick_s(base, peak)
  644.nab_s(base)
(Continued on next page)
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**SPEC CPU®2017 Floating Point Speed Result**

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Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
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C | 644.nab_s(peak)

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C++, C, Fortran | 607.cactuBSSN_s(base, peak)

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Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
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Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
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Fortran | 603.bwaves_s(base, peak) 649.fotonik3d_s(base, peak) 654.roms_s(base, peak)

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Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
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Fortran, C | 621.wrf_s(base, peak) 627.cam4_s(base, peak) 628.pop2_s(base, peak)

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Compiler Version Notes (Continued)

Base Compiler Invocation

C benchmarks:
icc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.caesarSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-m64 -std=c11 -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-mbranches-within-32B-boundaries

Fortran benchmarks:
-m64 -Wl,-z,muldefs -DSPEC_OPENMP -xCORE-AVX2 -ipo -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-nostandard-realloc-lhs -mbranches-within-32B-boundaries

(Continued on next page)
### Base Optimization Flags (Continued)

Fortran benchmarks (continued):

```
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
```

Benchmarks using both Fortran and C:

```
-m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX2 -ipo -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-DSPEC_OPENMP -mbranches-within-32B-boundaries -nostandard-realloc-lhs
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
```

Benchmarks using Fortran, C, and C++:

```
-m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX2 -ipo -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-DSPEC_OPENMP -mbranches-within-32B-boundaries -nostandard-realloc-lhs
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
```

### Peak Compiler Invocation

C benchmarks (except as noted below):

```
icc
```

```
644.nab_s: icx
```

Fortran benchmarks:

```
ifort
```

Benchmarks using both Fortran and C:

```
ifort icc
```

Benchmarks using Fortran, C, and C++:

```
icpc icc ifort
```

### Peak Portability Flags

Same as Base Portability Flags

### Peak Optimization Flags

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Silver 4316, 2.30GHz)

Peak Optimization Flags (Continued)

619.lbm_s: basepeak = yes

638.imagick_s: basepeak = yes

644.nab_s: -m64 -Wl,-z,muldefs -xCORE-AVX2 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -fioopenmp
-DSPEC_OPENMP -qopt-mem-layout-trans=4
-fimf-accuracy-bits=14:sqrt
-mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Fortran benchmarks:

603.bwaves_s: -m64 -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)
-DSPEC_SUPPRESS_OPENMP -DSPEC_OPENMP -ipo -xCORE-AVX2
-03 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -qopenmp -nostandard-realloc-lhs
-mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

649.fotonik3d_s: Same as 603.bwaves_s

654.roms_s: basepeak = yes

Benchmarks using both Fortran and C:

621.wrf_s: -m64 -std=c11 -Wl,-z,muldefs -prof-gen(pass 1)
-prof-use(pass 2) -ipo -xCORE-AVX2 -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

627.cam4_s: basepeak = yes

628.pop2_s: basepeak = yes

Benchmarks using Fortran, C, and C++:

607.cactuBSSN_s: basepeak = yes

The flags files that were used to format this result can be browsed at:
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<thead>
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**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Aug-2021  
**Hardware Availability:** Jun-2021  
**Software Availability:** Dec-2020

You can also download the XML flags sources by saving the following links:


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