Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6348, 2.60GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base =</th>
<th>388</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_fp_peak =</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Aug-2021  
**Hardware Availability:** Apr-2021  
**Software Availability:** Dec-2020

### Hardware

<table>
<thead>
<tr>
<th>Component</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Name</td>
<td>Intel Xeon Gold 6348</td>
</tr>
<tr>
<td>Max MHz</td>
<td>3500</td>
</tr>
<tr>
<td>Nominal</td>
<td>2600</td>
</tr>
<tr>
<td>Enabled</td>
<td>56 cores, 2 chips, 2 threads/core</td>
</tr>
<tr>
<td>Orderable</td>
<td>1,2 Chips</td>
</tr>
<tr>
<td>Cache L1</td>
<td>32 KB I + 48 KB D on chip per core</td>
</tr>
<tr>
<td>L2:</td>
<td>1.25 MB I+D on chip per core</td>
</tr>
<tr>
<td>L3:</td>
<td>42 MB I+D on chip per chip</td>
</tr>
<tr>
<td>Memory</td>
<td>2 TB (32 x 64 GB 2Rx4 PC4-3200V-R)</td>
</tr>
<tr>
<td>Storage</td>
<td>1 x 960 GB M.2 SSD SATA</td>
</tr>
<tr>
<td>Other</td>
<td>None</td>
</tr>
</tbody>
</table>

### Software

<table>
<thead>
<tr>
<th>Component</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS</td>
<td>SUSE Linux Enterprise Server 15 SP2 5.3.18-22-default</td>
</tr>
<tr>
<td>Compiler</td>
<td>C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux; Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux</td>
</tr>
<tr>
<td>Parallel</td>
<td>No</td>
</tr>
<tr>
<td>File System</td>
<td>btrfs</td>
</tr>
<tr>
<td>System State</td>
<td>Run level 3 (multi-user)</td>
</tr>
<tr>
<td>Base Pointers</td>
<td>64-bit</td>
</tr>
<tr>
<td>Peak Pointers</td>
<td>Not Applicable</td>
</tr>
<tr>
<td>Other</td>
<td>jemalloc memory allocator V5.0.1</td>
</tr>
<tr>
<td>Power Management</td>
<td>BIOS and OS set to prefer performance at the cost of additional power usage</td>
</tr>
</tbody>
</table>
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6348, 2.60GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
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SPECrate®2017_fp_base = 388
SPECrate®2017_fp_peak = Not Run

Results Table

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<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
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<td>503.bwaves_r</td>
<td>112</td>
<td>1547</td>
<td>726</td>
<td>1548</td>
<td>726</td>
<td>1550</td>
<td>725</td>
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<tr>
<td>507.cactuBSSN_r</td>
<td>112</td>
<td>266</td>
<td>534</td>
<td>264</td>
<td>537</td>
<td>266</td>
<td>534</td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>508.namd_r</td>
<td>112</td>
<td>343</td>
<td>310</td>
<td>344</td>
<td>309</td>
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<tr>
<td>510.parest_r</td>
<td>112</td>
<td>1456</td>
<td>201</td>
<td>1452</td>
<td>202</td>
<td>1446</td>
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<tr>
<td>511.povray_r</td>
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<td>454</td>
<td>577</td>
<td>453</td>
<td>575</td>
<td>454</td>
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<tr>
<td>519.lbm_r</td>
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<td>451</td>
<td>262</td>
<td>451</td>
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<tr>
<td>521.wrf_r</td>
<td>112</td>
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<td>736</td>
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<tr>
<td>526.blender_r</td>
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<tr>
<td>527.cam4_r</td>
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<td>470</td>
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<td>474</td>
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<tr>
<td>538.imagick_r</td>
<td>112</td>
<td>267</td>
<td>1040</td>
<td>258</td>
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<tr>
<td>544.nab_r</td>
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<tr>
<td>549.fotonik3d_r</td>
<td>112</td>
<td>1913</td>
<td>228</td>
<td>1913</td>
<td>228</td>
<td>1913</td>
<td>228</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>554.roms_r</td>
<td>112</td>
<td>1148</td>
<td>155</td>
<td>1144</td>
<td>156</td>
<td>1150</td>
<td>155</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOCCONF = "retain:true"

General Notes
Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6348, 2.60GHz)

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<td>Cisco Systems</td>
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<tr>
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<tr>
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<td>Dec-2020</td>
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</tbody>
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SPECraten®2017_fp_base = 388
SPECraten®2017_fp_peak = Not Run

General Notes (Continued)

sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numacl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDCS Sparing set to Disabled
Patrol Scrub set to Disabled
Processor C6 Report set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acfc64d running on install Sun Aug 22 11:21:39 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6348 CPU @ 2.60GHz
  2 "physical id"s (chips)
112 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 28
siblings : 56
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27

(Continued on next page)
### Cisco Systems

Cisco UCS B200 M6 (Intel Xeon Gold 6348, 2.60GHz)

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**SPEC CPU®2017 Floating Point Rate Result**

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<tbody>
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<td>SPECrate®2017_fp_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

**Platform Notes (Continued)**

From lscpu from util-linux 2.33.1:

- **Architecture**: x86_64
- **CPU op-mode(s)**: 32-bit, 64-bit
- **Byte Order**: Little Endian
- **Address sizes**: 46 bits physical, 57 bits virtual
- **CPU(s)**: 112
- **On-line CPU(s) list**: 0-111
- **Thread(s) per core**: 2
- **Core(s) per socket**: 28
- **Socket(s)**: 2
- **NUMA node(s)**: 4
- **Vendor ID**: GenuineIntel
- **CPU family**: 6
- **Model**: 106
- **Model name**: Intel(R) Xeon(R) Gold 6348 CPU @ 2.60GHz
- **Stepping**: 6
- **CPU MHz**: 3138.849
- **CPU max MHz**: 3500.0000
- **CPU min MHz**: 800.0000
- **BogoMIPS**: 5200.00
- **Virtualization**: VT-x
- **L1d cache**: 48K
- **L1i cache**: 32K
- **L2 cache**: 1280K
- **L3 cache**: 43008K
- **NUMA node0 CPU(s)**: 0-13, 56-69
- **NUMA node1 CPU(s)**: 14-27, 70-83
- **NUMA node2 CPU(s)**: 28-41, 84-97
- **NUMA node3 CPU(s)**: 42-55, 98-111
- **Flags**: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtrm pdcm pcid dca se4_1 se4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 invpcid_single ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vmi flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 3dnow invpcid rtm cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha ni avx512bw avx512vl xsaveopt xsaves xsavec xgetbv1 xsaveas cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local wbnoinvd dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkreq avx512vbmip umip pku ospke avx512_vbmi2 gfn vaes vpclmulqdq avx512_vnni avx512_bitalg tme avx512_vpopcntdq ia57 rdpid md_clear pconf lld arch_capabilities

/proc/cpuinfo cache data

- **cache size**: 43008 KB
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6348, 2.60GHz)

SPECrate®2017_fp_base = 388
SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2021
Hardware Availability: Apr-2021
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Platform Notes (Continued)

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 4 nodes (0-3)

node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 56 57 58 59 60 61 62 63 64 65 66 67 68 69
node 0 size: 515683 MB
node 0 free: 515198 MB

node 1 cpus: 14 15 16 17 18 19 20 21 22 23 24 25 26 27 70 71 72 73 74 75 76 77 78 79 80
81 82 83
node 1 size: 516088 MB
node 1 free: 515774 MB

node 2 cpus: 28 29 30 31 32 33 34 35 36 37 38 39 40 41 84 85 86 87 88 89 90 91 92 93 94
95 96 97
node 2 size: 516088 MB
node 2 free: 515788 MB

node 3 cpus: 42 43 44 45 46 47 48 49 50 51 52 53 54 55 98 99 100 101 102 103 104 105
106 107 108 109 110 111
node 3 size: 516051 MB
node 3 free: 515775 MB

node distances:

From /proc/meminfo
MemTotal: 2113446808 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*

os-release:
NAME="SLES"
VERSION="15-SP2"
VERSION_ID="15.2"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
Linux install 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
x86_64 x86_64 GNU/Linux

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6348, 2.60GHz)

SPECrate®2017_fp_base = 388
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

TEST RESULTS

Test Date: Aug-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Platform Notes (Continued)

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2018-3639 (Speculative Store Bypass): Mitigation: usercopy/swapgs barriers and __user pointer sanitization
CVE-2017-5753 (Spectre variant 1): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2017-5715 (Spectre variant 2): Not affected
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Aug 22 11:20
SPEC is set to: /home/cpu2017

<table>
<thead>
<tr>
<th>Filesystem</th>
<th>Type</th>
<th>Size</th>
<th>Used</th>
<th>Avail</th>
<th>Use%</th>
<th>Mounted on</th>
</tr>
</thead>
<tbody>
<tr>
<td>/dev/sda2</td>
<td>btrfs</td>
<td>892G</td>
<td>15G</td>
<td>875G</td>
<td>2%</td>
<td>/home</td>
</tr>
</tbody>
</table>

From /sys/devices/virtual/dmi/id
Vendor: Cisco Systems Inc
Product: UCSB-B200-M6
Serial: FCH24097578

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200

BIOS:
BIOS Vendor: Cisco Systems, Inc.
BIOS Version: B200M6.4.2.1d.0.0730210924
BIOS Date: 07/30/2021
BIOS Revision: 5.22

(End of data from sysinfo program)
# SPEC CPU®2017 Floating Point Rate Result

**Cisco Systems**

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**SPECrates**

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---

**Compiler Version Notes**

```plaintext
C
| 519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)
------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

C++
| 508.namd_r(base) 510.parest_r(base)
-------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

C++, C
| 511.povray_r(base) 526.blender_r(base)
---------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
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C++, C, Fortran
| 507.cactuBSSN_r(base)
-----------------------
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Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
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Fortran
| 503.bwaves_r(base) 549.fotonik3d_r(base) 554.roms_r(base)
--------------------------
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
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```

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Compiler Version Notes (Continued)

Fortran, C      | 521.wrf_r(base) 527.cam4_r(base)

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
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Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icx

Benchmarks using both C and C++:
icpx icx

Benchmarks using Fortran, C, and C++:
icpx icx ifort

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.1bm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char

(Continued on next page)
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527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
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544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

C++ benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Fortran benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
-qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using both Fortran and C:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using both C and C++:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using Fortran, C, and C++:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6348, 2.60GHz)

SPECrater®2017_fp_base = 388
SPECrater®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Aug-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Base Optimization Flags (Continued)

Benchmarks using Fortran, C, and C++ (continued):
- flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3
- no-prec-div -qopt-prefetch -ffinite-math-only
- qopt-multiple-gather-scatter-by-shuffles
- mbranches-within-32B-boundaries -nostandard-realloc-lhs
- align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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