## Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6338N, 2.20GHz)

<table>
<thead>
<tr>
<th>SPEC CPU®2017_fp_base</th>
<th>355</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPEC CPU®2017_fp_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Aug-2021  
**Hardware Availability:** Apr-2021  
**Software Availability:** Dec-2020

### Hardware
- **CPU Name:** Intel Xeon Gold 6338N  
- **Max MHz:** 3500  
- **Nominal:** 2200  
- **Enabled:** 64 cores, 2 chips, 2 threads/core  
- **Orderable:** 1,2 Chips  
- **Cache L1:** 32 KB I + 48 KB D on chip per core  
- **L2:** 1.25 MB I+D on chip per core  
- **L3:** 48 MB I+D on chip per chip  
- **Other:** None  
- **Memory:** 2 TB (32 x 64 GB 2Rx4 PC4-3200V-R, running at 2666)  
- **Storage:** 1 x 240 GB M.2 SSD SATA  
- **Other:** None

### Software
- **OS:** SUSE Linux Enterprise Server 15 SP2  
  5.3.18-22-default  
- **Compiler:** C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux; Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux  
- **Parallel:** No  
- **Firmware:** Version 4.2.1d released Jul-2021  
- **File System:** btrfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** Not Applicable  
- **Other:** jemalloc memory allocator V5.0.1  
- **Power Management:** BIOS and OS set to prefer performance at the cost of additional power usage

<table>
<thead>
<tr>
<th>Software</th>
<th>Hardware</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS:</td>
<td>CPU Name: Intel Xeon Gold 6338N</td>
</tr>
<tr>
<td></td>
<td>Max MHz: 3500</td>
</tr>
<tr>
<td></td>
<td>Nominal: 2200</td>
</tr>
<tr>
<td></td>
<td>Enabled: 64 cores, 2 chips, 2 threads/core</td>
</tr>
<tr>
<td></td>
<td>Orderable: 1,2 Chips</td>
</tr>
<tr>
<td></td>
<td>Cache L1: 32 KB I + 48 KB D on chip per core</td>
</tr>
<tr>
<td></td>
<td>L2: 1.25 MB I+D on chip per core</td>
</tr>
<tr>
<td></td>
<td>L3: 48 MB I+D on chip per chip</td>
</tr>
<tr>
<td></td>
<td>Other: None</td>
</tr>
<tr>
<td></td>
<td>Memory: 2 TB (32 x 64 GB 2Rx4 PC4-3200V-R, running at 2666)</td>
</tr>
<tr>
<td></td>
<td>Storage: 1 x 240 GB M.2 SSD SATA</td>
</tr>
<tr>
<td></td>
<td>Other: None</td>
</tr>
</tbody>
</table>

---

**Tested by:** Cisco Systems  
**Test Date:** Aug-2021  
**Hardware Availability:** Apr-2021  
**Software Availability:** Dec-2020

### Benchmark Results

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>128</td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>128</td>
</tr>
<tr>
<td>508.namd_r</td>
<td>128</td>
</tr>
<tr>
<td>510.parest_r</td>
<td>128</td>
</tr>
<tr>
<td>511.povray_r</td>
<td>128</td>
</tr>
<tr>
<td>519.lbm_r</td>
<td>128</td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>128</td>
</tr>
<tr>
<td>526.blender_r</td>
<td>128</td>
</tr>
<tr>
<td>527.cam4_r</td>
<td>128</td>
</tr>
<tr>
<td>538.imagick_r</td>
<td>128</td>
</tr>
<tr>
<td>544.nab_r</td>
<td>128</td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
<td>128</td>
</tr>
<tr>
<td>554.roms_r</td>
<td>128</td>
</tr>
</tbody>
</table>

**SPECrate®2017_fp_base (355)**
## SPEC CPU®2017 Floating Point Rate Result

**Cisco Systems**
Cisco UCS B200 M6 (Intel Xeon Gold 6338N, 2.20GHz)

### Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>128</td>
<td>2053</td>
<td>625</td>
<td>2052</td>
<td>626</td>
<td>2054</td>
<td>625</td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>128</td>
<td>322</td>
<td>503</td>
<td>323</td>
<td>502</td>
<td>326</td>
<td>498</td>
</tr>
<tr>
<td>508.namd_r</td>
<td>128</td>
<td>407</td>
<td>299</td>
<td>409</td>
<td>297</td>
<td>408</td>
<td>298</td>
</tr>
<tr>
<td>510.parest_r</td>
<td>128</td>
<td>1866</td>
<td>179</td>
<td>1868</td>
<td>179</td>
<td>1864</td>
<td>180</td>
</tr>
<tr>
<td>511.povray_r</td>
<td>128</td>
<td>681</td>
<td>439</td>
<td>684</td>
<td>437</td>
<td>682</td>
<td>438</td>
</tr>
<tr>
<td>519.lbm_r</td>
<td>128</td>
<td>590</td>
<td>229</td>
<td>589</td>
<td>229</td>
<td>590</td>
<td>229</td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>128</td>
<td>967</td>
<td>297</td>
<td>961</td>
<td>298</td>
<td>966</td>
<td>297</td>
</tr>
<tr>
<td>526.blender_r</td>
<td>128</td>
<td>490</td>
<td>398</td>
<td>486</td>
<td>401</td>
<td>488</td>
<td>400</td>
</tr>
<tr>
<td>527.cam4_r</td>
<td>128</td>
<td>564</td>
<td>397</td>
<td>564</td>
<td>397</td>
<td>567</td>
<td>395</td>
</tr>
<tr>
<td>538.imagick_r</td>
<td>128</td>
<td>310</td>
<td>1030</td>
<td>310</td>
<td>1030</td>
<td>317</td>
<td>1000</td>
</tr>
<tr>
<td>544.nab_r</td>
<td>128</td>
<td>321</td>
<td>671</td>
<td>325</td>
<td>663</td>
<td>324</td>
<td>664</td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
<td>128</td>
<td>2527</td>
<td>197</td>
<td>2525</td>
<td>198</td>
<td>2526</td>
<td>197</td>
</tr>
<tr>
<td>554.roms_r</td>
<td>128</td>
<td>1506</td>
<td>135</td>
<td>1501</td>
<td>136</td>
<td>1503</td>
<td>135</td>
</tr>
</tbody>
</table>

**SPECrate®2017_fp_base = 355**  
**SPECrate®2017_fp_peak = Not Run**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:  
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"  
MALLOC_CONF = "retain:true"

### General Notes

Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM  
memory using openSUSE Leap 15.2  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation  
Filesystem page cache synced and cleared with:

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6338N, 2.20GHz)

General Notes (Continued)

sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numacl i.e.:
numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.


Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDCS Sparing set to Disabled
Patrol Scrub set to Disabled
Processor C6 Report set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16aca64d64d
running on localhost Wed Aug 25 18:00:17 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

  model name : Intel(R) Xeon(R) Gold 6338N CPU @ 2.20GHz
  2 "physical id"s (chips)
  128 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 32
siblings : 64
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6338N, 2.20GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

From lscpu from util-linux 2.33.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 128
On-line CPU(s) list: 0-127
Thread(s) per core: 2
Core(s) per socket: 32
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Gold 6338N CPU @ 2.20GHz
Stepping: 6
CPU MHz: 2699.905
CPU max MHz: 3500.0000
CPU min MHz: 800.0000
BogoMIPS: 4400.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 128K
L3 cache: 49152K
NUMA node0 CPU(s): 0-15,64-79
NUMA node1 CPU(s): 16-31,80-95
NUMA node2 CPU(s): 32-47,96-111
NUMA node3 CPU(s): 48-63,112-127
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtrunc pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 invpcid_single ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vni flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ertz invvpid rtm cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha ni avx512bw avx512vl xsaves xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occmap llc cqm_mbmc_total cqm_mbmc_local wboinvd dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req avx512vmbi umip pku ospke avx512_vbmi2 gfnv vaes vpmulqdq avx512_vnni avx512_bitalg tme avx512_vpopcntdq 1a57 rdpid md_clear pconf gconf flush_lid arch_capabilities

/proc/cpuinfo cache data
  cache size : 49152 KB

(Continued on next page)
## SPEC CPU®2017 Floating Point Rate Result

**Cisco Systems**  
Cisco UCS B200 M6 (Intel Xeon Gold 6338N, 2.20GHz)  

- **CPU2017 License:** 9019  
- **Test Sponsor:** Cisco Systems  
- **Tested by:** Cisco Systems  
- **Test Date:** Aug-2021  
- **Hardware Availability:** Apr-2021  
- **Software Availability:** Dec-2020

### Platform Notes (Continued)

From `numactl --hardware`  
WARNING: a numactl 'node' might or might not correspond to a physical chip.  
available: 4 nodes (0-3)  
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79  
node 0 size: 515451 MB  
node 0 free: 515049 MB  
node 1 cpus: 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79  
node 1 size: 516088 MB  
node 1 free: 515634 MB  
node 2 cpus: 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79  
node 2 size: 516054 MB  
node 2 free: 515760 MB  
node 3 cpus: 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79  
node 3 size: 515808 MB  
node 3 free: 515540 MB  
node distances:  
node 0 1 2 3  
  0: 10 11 20 20  
  1: 11 10 20 20  
  2: 20 20 10 11  
  3: 20 20 11 10

From `/proc/meminfo`  
<table>
<thead>
<tr>
<th>Memory Usage</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>MemTotal</td>
<td>2112923596 kB</td>
</tr>
<tr>
<td>HugePages_Total</td>
<td>0</td>
</tr>
<tr>
<td>Hugepagesize</td>
<td>2048 kB</td>
</tr>
</tbody>
</table>

From `/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor`  
has performance

From `/etc/*release*` `/etc/*version*`  
```
os-release:
  NAME="SLES"
  VERSION="15-SP2"
  VERSION_ID="15.2"
  PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
  ID="sles"
  ID_LIKE="suse"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:15:sp2"
```

```
uname -a:  
Linux localhost 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
```
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6338N, 2.20GHz)

SPECrate®2017_fp_base = 355
SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Aug-2021
Tested by: Cisco Systems
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Platform Notes (Continued)

x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs barriers and __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Aug 25 17:52

SPEC is set to: /home/cpu2017

run-level 3 Aug 25 17:52

From /sys/devices/virtual/dmi/id
Vendor: Cisco Systems Inc
Product: UCSB-B200-M6
Serial: FCH24097576

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200, configured at 2666

BIOS:
BIOS Vendor: Cisco Systems, Inc.
BIOS Version: B200M6.4.2.id.0.0730210924
BIOS Date: 07/30/2021
BIOS Revision: 5.22

(End of data from sysinfo program)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6338N, 2.20GHz)

SPECrater®2017_fp_base = 355
SPECrater®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Compiler Version Notes

==============================================================================
<table>
<thead>
<tr>
<th>C</th>
<th>519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,</td>
<td></td>
</tr>
<tr>
<td>Version 2021.1 Build 20201113</td>
<td></td>
</tr>
<tr>
<td>Copyright (C) 1985-2020 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
<tr>
<td>------------------------------------------------------------------------------</td>
<td></td>
</tr>
</tbody>
</table>

==============================================================================
<table>
<thead>
<tr>
<th>C++</th>
<th>508.namd_r(base) 510.parest_r(base)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,</td>
<td></td>
</tr>
<tr>
<td>Version 2021.1 Build 20201113</td>
<td></td>
</tr>
<tr>
<td>Copyright (C) 1985-2020 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
<tr>
<td>------------------------------------------------------------------------------</td>
<td></td>
</tr>
</tbody>
</table>

==============================================================================
<table>
<thead>
<tr>
<th>C++, C</th>
<th>511.povray_r(base) 526.blender_r(base)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,</td>
<td></td>
</tr>
<tr>
<td>Version 2021.1 Build 20201113</td>
<td></td>
</tr>
<tr>
<td>Copyright (C) 1985-2020 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
<tr>
<td>Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,</td>
<td></td>
</tr>
<tr>
<td>Version 2021.1 Build 20201113</td>
<td></td>
</tr>
<tr>
<td>Copyright (C) 1985-2020 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
<tr>
<td>------------------------------------------------------------------------------</td>
<td></td>
</tr>
</tbody>
</table>

==============================================================================
<table>
<thead>
<tr>
<th>C++, C, Fortran</th>
<th>507.cactuBSSN_r(base)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,</td>
<td></td>
</tr>
<tr>
<td>Version 2021.1 Build 20201113</td>
<td></td>
</tr>
<tr>
<td>Copyright (C) 1985-2020 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
<tr>
<td>Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,</td>
<td></td>
</tr>
<tr>
<td>Version 2021.1 Build 20201113</td>
<td></td>
</tr>
<tr>
<td>Copyright (C) 1985-2020 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
<tr>
<td>------------------------------------------------------------------------------</td>
<td></td>
</tr>
</tbody>
</table>

==============================================================================
<table>
<thead>
<tr>
<th>Fortran</th>
<th>503.bwaves_r(base) 549.fotonik3d_r(base) 554.roms_r(base)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on</td>
<td></td>
</tr>
<tr>
<td>Intel(R) 64, Version 2021.1 Build 20201112_000000</td>
<td></td>
</tr>
<tr>
<td>Copyright (C) 1985-2020 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
<tr>
<td>------------------------------------------------------------------------------</td>
<td></td>
</tr>
</tbody>
</table>

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6338N, 2.20GHz)

SPEC CPU®2017 Floating Point Rate Result
Copyright 2017-2021 Standard Performance Evaluation Corporation

Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6338N, 2.20GHz)

<table>
<thead>
<tr>
<th>CPU2017 License: 9019</th>
<th>Test Date: Aug-2021</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor: Cisco Systems</td>
<td>Hardware Availability: Apr-2021</td>
</tr>
<tr>
<td>Tested by: Cisco Systems</td>
<td>Software Availability: Dec-2020</td>
</tr>
</tbody>
</table>

**Compiler Version Notes (Continued)**

Fortran, C      | 521.wrf_r(base) 527.cam4_r(base)
----------------|---------------------------------------------------------

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

**Base Compiler Invocation**

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icx

Benchmarks using both C and C++:
icpx icx

Benchmarks using Fortran, C, and C++:
icpx icx ifort

**Base Portability Flags**

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6338N, 2.20GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base</th>
<th>355</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_fp_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Base Portability Flags (Continued)

527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

C++ benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Fortran benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
-qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using both Fortran and C:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-nostandard-realloc-lhs -align array32byte -auto -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using both C and C++:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using Fortran, C, and C++:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6338N, 2.20GHz)

SPECrater®2017_fp_base = 355
SPECrater®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Base Optimization Flags (Continued)

Benchmarks using Fortran, C, and C++ (continued):
-fflto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml

SPEC CPU and SPECrater are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.8 on 2021-08-25 21:00:16-0400.
Originally published on 2021-09-14.