Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 5320T, 2.30GHz)

SPECrater®2017_int_base = 276
SPECrater®2017_int_peak = 285

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

500.perlbench_r 80
502.gcc_r 80
505.mcf_r 80
520.omnetpp_r 80
523.xalancbmk_r 80
525.x264_r 80
531.deepsjeng_r 80
541.leela_r 80
548.exchange2_r 80
557.xz_r 80

<table>
<thead>
<tr>
<th>Software</th>
<th>Hardware</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS: SUSE Linux Enterprise Server 15 SP2</td>
<td>CPU Name: Intel Xeon Gold 5320T</td>
</tr>
<tr>
<td>Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux; Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux; C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux</td>
<td>Max MHz: 3500</td>
</tr>
<tr>
<td>Firmware: Version 4.2.1d released Jul-2021</td>
<td>Nominal: 2300</td>
</tr>
<tr>
<td>File System: btrfs</td>
<td>Enabled: 40 cores, 2 chips, 2 threads/core</td>
</tr>
<tr>
<td>System State: Run level 3 (multi-user)</td>
<td>Orderable: 1,2 Chips</td>
</tr>
<tr>
<td>Base Pointers: 64-bit</td>
<td>Cache L1: 32 KB I + 48 KB D on chip per core</td>
</tr>
<tr>
<td>Peak Pointers: 32/64-bit</td>
<td>L2: 1.25 MB I+D on chip per core</td>
</tr>
<tr>
<td>Other: jemalloc memory allocator V5.0.1</td>
<td>L3: 30 MB I+D on chip per chip</td>
</tr>
<tr>
<td>Power Management: BIOS and OS set to prefer performance at the cost of additional power usage</td>
<td>Other: None</td>
</tr>
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Hardware
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Nominal: 2300
Enabled: 40 cores, 2 chips, 2 threads/core
Orderable: 1,2 Chips
Cache L1: 32 KB I + 48 KB D on chip per core
L2: 1.25 MB I+D on chip per core
L3: 30 MB I+D on chip per chip
Other: None
Memory: 2 TB (32 x 64 GB 2Rx4 PC4-3200V-R, running at 2933)
Storage: 1 x 240 GB M.2 SSD SATA
Other: None
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 5320T, 2.30GHz)

CPU2017 License: 9019
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Results Table

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<th>Benchmark</th>
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<td>560</td>
<td>154</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH =
    "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

MALLOC_CONF = "retain:true"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
    sync; echo 3> /proc/sys/vm/drop_caches

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 5320T, 2.30GHz)

**SPEC CPU®2017 Integer Rate Result**

**SPECrate**

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<th><strong>SPECrate®2017_int_base</strong></th>
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<td><strong>SPECrate®2017_int_peak</strong></td>
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**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Aug-2021

**Hardware Availability:** Apr-2021

**Software Availability:** Dec-2020

---

**General Notes (Continued)**

runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.


---

**Platform Notes**

**BIOS Settings:**
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
UPI Link Enablement set to 1
UPI Power Management set to Enabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDDC Sparing set to Disabled
Patrol Scrub set to Disabled
Energy Efficient Turbo set to Enabled
Processor C6 Report set to Enabled
Processor C1E set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d
running on localhost Fri Aug 27 04:19:11 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 5320T CPU @ 2.30GHz
  2 "physical id"s (chips)
  80 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 20
siblings : 40
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 5320T, 2.30GHz)

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<tbody>
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</tr>
</tbody>
</table>

**Platform Notes (Continued)**

From `lscpu` from `util-linux 2.33.1`:
- **Architecture**: x86_64
- **CPU op-mode(s)**: 32-bit, 64-bit
- **Byte Order**: Little Endian
- **Address sizes**: 46 bits physical, 57 bits virtual
- **CPU(s)**: 80
- **On-line CPU(s) list**: 0-79
- **Thread(s) per core**: 2
- **Core(s) per socket**: 20
- **Socket(s)**: 2
- **NUMA node(s)**: 4
- **Vendor ID**: GenuineIntel
- **CPU family**: 6
- **Model**: 106
- **Model name**: Intel(R) Xeon(R) Gold 5320T CPU @ 2.30GHz
- **Stepping**: 6
- **CPU MHz**: 801.426
- **CPU max MHz**: 3500.0000
- **CPU min MHz**: 800.0000
- **BogoMIPS**: 4600.00
- **Virtualization**: VT-x
- **L1d cache**: 48K
- **L1i cache**: 32K
- **L2 cache**: 1280K
- **L3 cache**: 30720K
- **NUMA node0 CPU(s)**: 0-9, 40-49
- **NUMA node1 CPU(s)**: 10-19, 50-59
- **NUMA node2 CPU(s)**: 20-29, 60-69
- **NUMA node3 CPU(s)**: 30-39, 70-79
- **Flags**: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 invpcid_single ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd shani avx512bw avx512vl xsaveset xsaves xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local wbinvd dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req avx512vmbmi umip pku ospke avx512_vbmi2 gfnv vaes vpcpumulqdq avx512_vnni avx512_bitalg tme avx512_vpopcntdq la57 rdpid md_clear pconfig flush_l1d arch_capabilities

/proc/cpuinfo cache data
cache size : 30720 KB

(Continued on next page)
From `numactl --hardware`
WARNING: a `numactl 'node'` might or might not correspond to a physical chip.
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 40 41 42 43 44 45 46 47 48 49
node 0 size: 515420 MB
node 0 free: 515135 MB
node 1 cpus: 10 11 12 13 14 15 16 17 18 19 50 51 52 53 54 55 56 57 58 59
node 1 size: 516090 MB
node 1 free: 515737 MB
node 2 cpus: 20 21 22 23 24 25 26 27 28 29 60 61 62 63 64 65 66 67 68 69
node 2 size: 516090 MB
node 2 free: 515773 MB
node 3 cpus: 30 31 32 33 34 35 36 37 38 39 70 71 72 73 74 75 76 77 78 79
node 3 size: 515810 MB
node 3 free: 515493 MB
node distances:
node 0 1 2 3
0: 10 11 20 20
1: 11 10 20 20
2: 20 20 10 11
3: 20 20 11 10

From `/proc/meminfo`
MemTotal: 2112934360 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From `/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor` has performance

From `/etc/*release* /etc/*version*`
os-release:
NAME="SLES"
VERSION="15-SP2"
VERSION_ID="15.2"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp2"

`uname -a`:
Linux localhost 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

(Continued on next page)
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Platform Notes (Continued)

CVE-2018-12207 (ITLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2018-3639 (Speculative Store Bypass): Mitigation: usercopy/swapgs barriers and __user pointer sanitization

CVE-2017-5753 (Spectre variant 1):
CVE-2017-5715 (Spectre variant 2):
CVE-2020-0543 (Special Register Buffer Data Sampling):
CVE-2019-11135 (TSX Asynchronous Abort):

run-level 3 Aug 27 04:17

SPEC is set to: /home/cpu2017
From /sys/devices/virtual/dmi/id
Vendor: Cisco Systems Inc
Product: UCSB-B200-M6
Serial: FCH24097576

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200, configured at 2933

BIOS:
BIOS Vendor: Cisco Systems, Inc.
BIOS Version: B200M6.4.2.1d.0.0730210924
BIOS Date: 07/30/2021
BIOS Revision: 5.22

(End of data from sysinfo program)

Compiler Version Notes

C | 500.perlbench_r(peak) 557.xz_r(peak)

(Continued on next page)
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**Compiler Version Notes (Continued)**

| C | 502.gcc_r(peak) |
| Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version 2021.1 Build 20201113 |
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

| C | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak) 525.x264_r(base, peak) 557.xz_r(base) |
| Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113 |
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

| C | 500.perlbench_r(peak) 557.xz_r(peak) |
| Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000 |
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

| C | 502.gcc_r(peak) |
| Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version 2021.1 Build 20201113 |
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| C | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak) 525.x264_r(base, peak) 557.xz_r(base) |
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## Compiler Version Notes (Continued)

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Base Compiler Invocation

C benchmarks:
icx

c++ benchmarks:
icpx

Fortran benchmarks:
ifort

Base Portability Flags

500.perlibench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

C++ benchmarks:
-wm64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

Fortran benchmarks:
-wm64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-auto -mbranches-within-32B-boundaries

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 5320T, 2.30GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base = 276</th>
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<td>SPECrate®2017_int_peak = 285</td>
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**CPU2017 License:** 9019
**Test Sponsor:** Cisco Systems
**Test Date:** Aug-2021
**Hardware Availability:** Apr-2021
**Tested by:** Cisco Systems
**Software Availability:** Dec-2020

### Base Optimization Flags (Continued)

Fortran benchmarks (continued):
- `-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin`
- `-lqkmalloc`

### Peak Compiler Invocation

C benchmarks (except as noted below):
- `icx`
- `500.perlbench_r: icc`
- `557.xz_r: icc`

C++ benchmarks:
- `icpx`

Fortran benchmarks:
- `ifort`

### Peak Portability Flags

- `500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64`
- `502.gcc_r: -D_FILE_OFFSET_BITS=64`
- `505.mcf_r: -DSPEC_LP64`
- `520.omnetpp_r: -DSPEC_LP64`
- `523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX`
- `525.x264_r: -DSPEC_LP64`
- `531.deepsjeng_r: -DSPEC_LP64`
- `541.leela_r: -DSPEC_LP64`
- `548.exchange2_r: -DSPEC_LP64`
- `557.xz_r: -DSPEC_LP64`

### Peak Optimization Flags

C benchmarks:
- `500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)
-xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-strict-overflow
-mbranches-within-32B-boundaries`

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Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 5320T, 2.30GHz)

**SPEC CPU®2017 Integer Rate Result**

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**Peak Optimization Flags (Continued)**

500.perlbench_r (continued):
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

502.gcc_r: -m32
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/ia32_lin
-std=gnu89 -Wl,-z,muldefs -fprofile-generate(pass1)
-fprofile-use=default.profdata(pass2) -xCORE-AVX512 -flto
-Ofast(pass1) -O3 -ffast-math -qopt-mem-layout-trans=4
-mbranches-within-32B-bounds
-L/usr/local/jemalloc32-5.0.1/lib -ljemalloc

505.mcf_r: basepeak = yes

525.x264_r: -w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -flto
-O3 -ffast-math -qopt-mem-layout-trans=4 -fno-alias
-mbranches-within-32B-bounds
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

557.xz_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -mbranches-within-32B-bounds
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

C++ benchmarks:
520.omnetpp_r: basepeak = yes
523.xalancbmk_r: basepeak = yes
531.deepsjeng_r: basepeak = yes
541.leela_r: basepeak = yes

Fortran benchmarks:
548.exchange2_r: basepeak = yes

The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:

http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml
# SPEC CPU®2017 Integer Rate Result

## Cisco Systems

Cisco UCS B200 M6 (Intel Xeon Gold 5320T, 2.30GHz)  

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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