## SPEC CPU®2017 Floating Point Speed Result

Hewlett Packard Enterprise  
(Test Sponsor: HPE)  
ProLiant DL380 Gen10 Plus  
(2.40 GHz, Intel Xeon Gold 6312U)  

| SPECspeed®2017_fp_base | 121 |
| SPECspeed®2017_fp_peak | 123 |

### Hardware
- CPU Name: Intel Xeon Gold 6312U
- Max MHz: 3600
- Nominal: 2400
- Enabled: 24 cores, 1 chip
- Orderable: 1, 2 chip(s)
- Cache L1: 32 KB I + 48 KB D on chip per core
- L2: 1.25 MB I+D on chip per core
- L3: 36 MB I+D on chip per chip
- Other: None
- Memory: 1 TB (16 x 64 GB 2Rx4 PC4-3200AA-A-R)
- Storage: 1 x 400 GB SAS SSD, RAID 0
- Other: None

### Software
- OS: Red Hat Enterprise Linux 8.3 (Ootpa)
- Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux; Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux; C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux
- Parallel: Yes
- Firmware: HPE BIOS Version U46 v1.50 05/27/2021 released May-2021
- File System: xfs
- System State: Run level 3 (multi-user)
- Base Pointers: 64-bit
- Peak Pointers: 64-bit
- Power Management: BIOS set to prefer performance at the cost of additional power usage

### Test Result

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Specspeed®2017_fp_peak</th>
<th>Specspeed®2017_fp_base</th>
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<tbody>
<tr>
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<td>628.pop2_s</td>
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SPECspeed®2017_fp_base = 121
SPECspeed®2017_fp_peak = 123

Results Table

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SPECspeed®2017_fp_base = 121
SPECspeed®2017_fp_peak = 123

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
    sync; echo 3> /proc/sys/vm/drop_caches

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
    KMP_AFFINITY = "granularity=fine,compact"
    LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
    MALLOC_CONF = "retain:true"
    OMP_STACKSIZE = "192M"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM memory using Redhat Enterprise Linux 8.0
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
    built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

(Continued on next page)
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SPECspeed®2017_fp_base = 121
SPECspeed®2017_fp_peak = 123

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Test Date: Aug-2021
Hardware Availability: Jun-2021
Software Availability: Dec-2020

General Notes (Continued)


Platform Notes

The system ROM used for this result contains Intel microcode version 0xd0002a0 for the Intel Xeon Gold 6312U processor

BIOS Configuration:

- Workload Profile set to General Peak Frequency Compute
- Intel Hyper-Threading set to Disabled
- Thermal Configuration set to Maximum Cooling
- Memory Patrol Scrubbing set to Disabled
- Advanced Memory Protection set to Advanced ECC
- Last Level Cache (LLC) Prefetch set to Enabled
- Last Level Cache (LLC) Dead Line Allocation set to Disabled
- Enhanced Processor Performance set to Enabled
- Workload Profile set to Custom
  - Energy/Performance Bias set to Balanced Power
  - DCU Stream Prefetcher set to Disabled
  - Adjacent Sector Prefetch set to Disabled
  - Minimum Processor Idle Power Package C-State set to No Package State
  - Numa Group Size Optimization set to Flat

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16aca6c64d
running on localhost.localdomain Wed Aug 18 09:00:05 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

- model name : Intel(R) Xeon(R) Gold 6312U CPU @ 2.40GHz
- 1 "physical id"s (chips)
- 24 "processors"

cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
- cpu cores : 24
- siblings : 24
- physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23

From lscpu from util-linux 2.32.1:
- Architecture: x86_64
- CPU op-mode(s): 32-bit, 64-bit
- Byte Order: Little Endian
- CPU(s): 24
- On-line CPU(s) list: 0-23

(Continued on next page)
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Platform Notes (Continued)

Thread(s) per core: 1
Core(s) per socket: 24
Socket(s): 1
NUMA node(s): 1
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Gold 6312U CPU @ 2.40GHz
Stepping: 6
CPU MHz: 3472.226
BogoMIPS: 4800.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 36864K
NUMA node0 CPU(s): 0-23

Flags: fpu vme de pse tsc msr pae mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lmlahf_lm dtes64e monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lmlahf_lm dtes64e monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lmlahf_lm dtes64e monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lmlahf_lm dtes64e monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lmlahf_lm dtes64e monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 1 nodes (0)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
node 0 size: 980701 MB
node 0 free: 1023996 MB
node distances:
node 0
0: 10

From /proc/meminfo
MemTotal: 1056534488 KB
HugePages_Total: 0

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SPECspeed®2017_fp_base = 121
SPECspeed®2017_fp_peak = 123

Platform Notes (Continued)

\textit{Hugepagesize:} 2048 kB

/sbin/tuned-adm active
Current active profile: throughput-performance

\textit{From} /etc/*release*/etc/*version*
\textit{os-release:}
NAME="Red Hat Enterprise Linux"
VERSION="8.3 (Ootpa)"
ID="rhel"
ID_LIKE="fedora"
VERSION_ID="8.3"
PLATFORM_ID="platform:el8"
PRETTY_NAME="Red Hat Enterprise Linux 8.3 (Ootpa)"
ANSI_COLOR="0;31"

\textit{redhat-release}: Red Hat Enterprise Linux release 8.3 (Ootpa)
\textit{system-release}: Red Hat Enterprise Linux release 8.3 (Ootpa)
\textit{system-release-cpe}: cpe:/o:redhat:enterprise_linux:8.3:ga

\texttt{uname -a:}
Linux localhost.localdomain 4.18.0-240.el8.x86_64 #1 SMP Wed Sep 23 05:13:10 EDT 2020
x86_64 x86_64 x86_64 GNU/Linux

\textit{Kernel self-reported vulnerability status:}

\textbf{CVE-2018-12207 (iTLB Multihit):} Not affected

\textbf{CVE-2018-3620 (L1 Terminal Fault):} Not affected

\textbf{Microarchitectural Data Sampling:} Not affected

\textbf{CVE-2017-5754 (Meltdown):} Not affected

\textbf{CVE-2018-3639 (Speculative Store Bypass):} Mitigation: Speculative Store Bypass disabled via prctl and seccomp

\textbf{CVE-2017-5753 (Spectre variant 1):} Mitigation: usercopy/swaps barriers and __user pointer sanitization

\textbf{CVE-2017-5715 (Spectre variant 2):} Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

\textbf{CVE-2020-0543 (Special Register Buffer Data Sampling):} Not affected

\textbf{CVE-2019-11135 (TSX Asynchronous Abort):} Not affected

\textit{run-level 3 Aug 18 05:08}

\textit{SPEC is set to:} /home/cpu2017
\textit{Filesystem} Type Size Used Avail Use% Mounted on
/devmapper/rhel-home xfs 297G 103G 195G 35% /home

\textit{From} /sys/devices/virtual/dmi/id

\textbf{(Continued on next page)}
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Test Sponsor: HPE  
Tested by: HPE  

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Test Date: Aug-2021  
Hardware Availability: Jun-2021  
Software Availability: Dec-2020

Platform Notes (Continued)

Vendor: HPE  
Product: ProLiant DL380 Gen10 Plus  
Product Family: ProLiant  
Serial: CN70110BZV

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
16x Micron 36ASF8G72PZ-3G2B2 64 GB 2 rank 3200  
16x UNKNOWN NOT AVAILABLE

BIOS:
BIOS Vendor: HPE  
BIOS Version: U46  
BIOS Date: 05/27/2021  
BIOS Revision: 1.50  
Firmware Revision: 2.50

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
| C               | 619.lbm_s(base, peak) 638.imagick_s(base, peak) 644.nab_s(base) |
==============================================================================

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================

| C               | 644.nab_s(peak) |
==============================================================================

Intel(R) oneAPI DPC+/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================

| C               | 619.lbm_s(base, peak) 638.imagick_s(base, peak) 644.nab_s(base) |
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Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
Compiler Version Notes (Continued)

64, Version 2021.1 Build 20201112_000000
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C               | 644.nab_s(peak)
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C++, C, Fortran | 607.cactuBSSN_s(base, peak)
Intel(R) C++ Intel(R) 64 Compiler Classic for applications running on
   Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
   64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
   Intel(R) 64, Version 2021.1 Build 20201112_000000
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==============================================================================
Fortran         | 603.bwaves_s(base, peak) 649.fotonik3d_s(base, peak)
   654.roms_s(base, peak)
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
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Copyright 2017-2021 Standard Performance Evaluation Corporation

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Base Compiler Invocation

C benchmarks:
icc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-m64 -std=c11 -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -gopenmp -DSPEC_OPENMP
-mbranches-within-32B-boundaries

Fortran benchmarks:
-m64 -Wl,-z,muldefs -DSPEC_OPENMP -xCORE-AVX512 -ipo -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -gopenmp -nostandard-realloc-lhs
-mbranches-within-32B-boundaries -L/usr/local/jemalloc64-5.0.1/lib
-ljemalloc

Benchmarks using both Fortran and C:
-m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div

(Continued on next page)
## Base Optimization Flags (Continued)

Benchmarks using both Fortran and C (continued):
- `-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp`
- `-DSPEC_OPENMP -mbranches-within-32B-boundaries -nostandard-realloc-lhs`
- `-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc`

Benchmarks using Fortran, C, and C++:
- `-m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
- `-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp`
- `-DSPEC_OPENMP -mbranches-within-32B-boundaries -nostandard-realloc-lhs`
- `-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc`

## Peak Compiler Invocation

C benchmarks (except as noted below):
```
icc
```

For Fortran benchmarks:
```
ifort
```

Benchmarks using both Fortran and C:
```
ifort icc
```

Benchmarks using Fortran, C, and C++:
```
icpc icc ifort
```

## Peak Portability Flags

Same as Base Portability Flags

## Peak Optimization Flags

C benchmarks:
```
619.lbm_s: basepeak = yes
```
```
638.imagick_s: basepeak = yes
```

(Continued on next page)
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CPU2017 License: 3
Test Sponsor: HPE
Test Date: Aug-2021
Tested by: HPE
Hardware Availability: Jun-2021
Software Availability: Dec-2020

Peak Optimization Flags (Continued)

644.nab_s: -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-fflt -mfpmath=sse -funroll-loops -floop-lmis
-DSPEC_OPENMP -qopt-mem-layout-trans=4
-flto -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Fortran benchmarks:

603.bwaves_s: -m64 -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)
-DSPEC_SUPPRESS_OPENMP -DSPEC_OPENMP -ipo -xCORE-AVX512
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -qopenmp -nostandard-realloc-lhs
-mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

649.fotonik3d_s: Same as 603.bwaves_s

654.roms_s: basepeak = yes

Benchmarks using both Fortran and C:

621.wrf_s: -m64 -std=c11 -Wl,-z,muldefs -prof-gen(pass 1)
-prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

627.cam4_s: basepeak = yes

628.pop2_s: basepeak = yes

Benchmarks using Fortran, C, and C++:

607.cactuBSSN_s: basepeak = yes

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.0-ICX-revE.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.0-ICX-revE.xml
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml
Hewlett Packard Enterprise
(Test Sponsor: HPE)
ProLiant DL380 Gen10 Plus
(2.40 GHz, Intel Xeon Gold 6312U)

<table>
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SPECspeed\textsuperscript{®}2017\_fp\_base = 121
SPECspeed\textsuperscript{®}2017\_fp\_peak = 123

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU\textsuperscript{®}2017 v1.1.8 on 2021-08-17 23:30:04-0400.
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