



# SPEC CPU®2017 Floating Point Speed Result

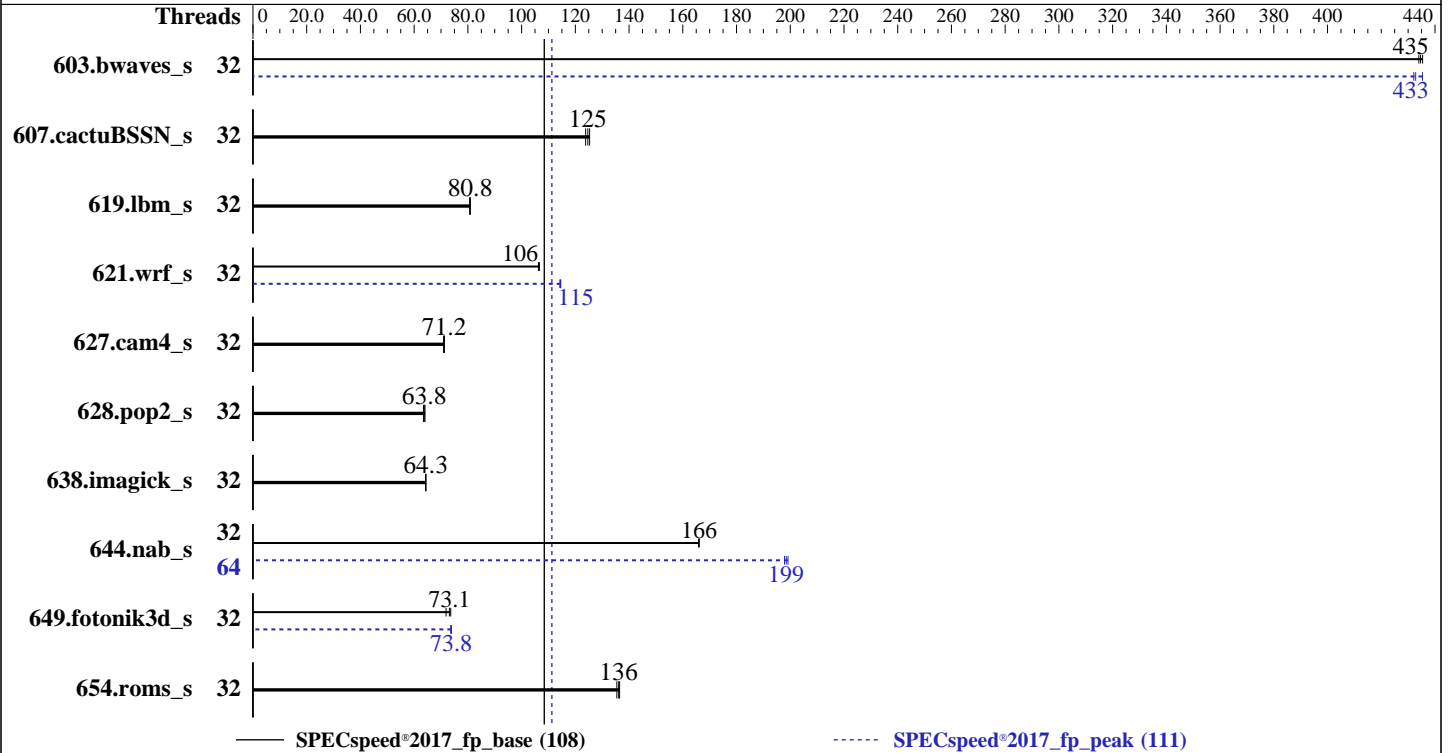
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**Tyrone Systems**  
(Test Sponsor: Netweb Pte Ltd)  
Tyrone Camarero DIT400TR-48RL  
(2.10 GHz, Intel Xeon Silver 4216)

SPECspeed®2017\_fp\_base = 108  
SPECspeed®2017\_fp\_peak = 111

CPU2017 License: 006042  
Test Sponsor: Netweb Pte Ltd  
Tested by: Tyrone Systems

Test Date: Aug-2021  
Hardware Availability: Apr-2019  
Software Availability: Jun-2021



## Hardware

CPU Name: Intel Xeon Silver 4216  
Max MHz: 3200  
Nominal: 2100  
Enabled: 32 cores, 2 chips, 2 threads/core  
Orderable: 1,2 Chips  
Cache L1: 32 KB I + 32 KB D on chip per core  
L2: 1 MB I+D on chip per core  
L3: 22 MB I+D on chip per chip  
Other: None  
Memory: 384 GB (12 x 32 GB 2Rx4 PC4-2933P-R, running at 2400)  
Storage: 1 x 480 GB SATA SSD  
Other: None

## Software

OS: CentOS Linux release 8.4.2105  
Kernel 4.18.0-305.3.1.el8.x86\_64  
Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux;  
Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux;  
C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux  
Parallel: Yes  
Firmware: Version V8.104 released Jul-2021  
File System: xfs  
System State: Run level 3 (multi-user)  
Base Pointers: 64-bit  
Peak Pointers: 64-bit  
Other: jemalloc memory allocator V5.0.1  
Power Management: BIOS set to prefer performance at the cost of additional power usage.



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## Results Table

Benchmark	Base						Peak							
	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
603.bwaves_s	32	136	435	136	434	<b>136</b>	<b>435</b>	32	<b>136</b>	<b>433</b>	137	432	136	435
607.cactuBSSN_s	32	<b>134</b>	<b>125</b>	135	124	133	125	32	<b>134</b>	<b>125</b>	135	124	133	125
619.lbm_s	32	<b>64.8</b>	<b>80.8</b>	64.9	80.7	64.8	80.9	32	<b>64.8</b>	<b>80.8</b>	64.9	80.7	64.8	80.9
621.wrf_s	32	<b>124</b>	<b>106</b>	124	106	124	107	32	<b>115</b>	<b>115</b>	116	114	115	115
627.cam4_s	32	124	71.2	125	71.0	<b>124</b>	<b>71.2</b>	32	124	71.2	125	71.0	<b>124</b>	<b>71.2</b>
628.pop2_s	32	187	63.5	185	64.0	<b>186</b>	<b>63.8</b>	32	187	63.5	185	64.0	<b>186</b>	<b>63.8</b>
638.imagick_s	32	225	64.2	<b>224</b>	<b>64.3</b>	224	64.4	32	225	64.2	<b>224</b>	<b>64.3</b>	224	64.4
644.nab_s	32	105	166	105	166	<b>105</b>	<b>166</b>	64	87.7	199	88.3	198	<b>88.0</b>	<b>199</b>
649.fotonik3d_s	32	124	73.6	127	71.9	<b>125</b>	<b>73.1</b>	32	124	73.6	<b>124</b>	<b>73.8</b>	123	73.8
654.roms_s	32	115	136	116	135	<b>116</b>	<b>136</b>	32	115	136	116	135	<b>116</b>	<b>136</b>

SPECSpeed®2017\_fp\_base = **108**

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## Environment Variables Notes

Environment variables set by runcpu before the start of the run:  
KMP\_AFFINITY = "granularity=fine,compact,1,0"  
LD\_LIBRARY\_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"  
MALLOC\_CONF = "retain:true"  
OMP\_STACKSIZE = "192M"

## General Notes

Binaries compiled locally by Netweb  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation  
Filesystem page cache synced and cleared with:  
sync; echo 3> /proc/sys/vm/drop\_caches  
runcpu command invoked through numactl i.e.:  
numactl --interleave=all runcpu <etc>

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## General Notes (Continued)

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation

built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>

## Platform Notes

BIOS Settings:

Power Technology set to Custom

Power Performance Tuning set to BIOS Controls EPB

ENERGY\_PERF\_BIAS\_CFG mode set to Performance

LLC Dead Line Alloc set to Disable

sysinfo program /home/cpu2017/bin/sysinfo

Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d

running on localhost.localdomain Mon Aug 9 05:35:21 2021

SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see

<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Silver 4216 CPU @ 2.10GHz

2 "physical id"s (chips)

64 "processors"

cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

cpu cores : 16

siblings : 32

physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lscpu from util-linux 2.32.1:

Architecture: x86\_64

CPU op-mode(s): 32-bit, 64-bit

Byte Order: Little Endian

CPU(s): 64

On-line CPU(s) list: 0-63

Thread(s) per core: 2

Core(s) per socket: 16

(Continued on next page)



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## Platform Notes (Continued)

```

Socket(s):                2
NUMA node(s):             2
Vendor ID:                GenuineIntel
BIOS Vendor ID:          Intel(R) Corporation
CPU family:               6
Model:                   85
Model name:               Intel(R) Xeon(R) Silver 4216 CPU @ 2.10GHz
BIOS Model name:         Intel(R) Xeon(R) Silver 4216 CPU @ 2.10GHz
Stepping:                 7
CPU MHz:                  800.081
CPU max MHz:              3200.0000
CPU min MHz:              800.0000
BogoMIPS:                 4200.00
Virtualization:           VT-x
L1d cache:                32K
L1i cache:                32K
L2 cache:                 1024K
L3 cache:                 22528K
NUMA node0 CPU(s):       0-15,32-47
NUMA node1 CPU(s):       16-31,48-63
Flags:                    fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx fl6c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3
invpcid_single intel_ppin ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi
flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms
invpcid cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt
avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc
cqm_mbm_total cqm_mbm_local dtherm ida arat pln pts hwp hwp_act_window hwp_epp
hwp_pkg_req pku ospke avx512_vnni md_clear flush_lld arch_capabilities

```

```

/proc/cpuinfo cache data
cache size : 22528 KB

```

From numactl --hardware

WARNING: a numactl 'node' might or might not correspond to a physical chip.

available: 2 nodes (0-1)

node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 32 33 34 35 36 37 38 39 40 41 42 43  
44 45 46 47

node 0 size: 192106 MB

node 0 free: 166784 MB

node 1 cpus: 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 48 49 50 51 52 53 54 55 56  
57 58 59 60 61 62 63

node 1 size: 193491 MB

node 1 free: 168760 MB

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## Platform Notes (Continued)

node distances:

```
node 0 1
0: 10 21
1: 21 10
```

From /proc/meminfo

```
MemTotal: 394851992 kB
HugePages_Total: 0
Hugepagesize: 2048 kB
```

/sbin/tuned-adm active

Current active profile: throughput-performance

/sys/devices/system/cpu/cpu\*/cpufreq/scaling\_governor has  
performance

From /etc/\*release\* /etc/\*version\*

```
centos-release: CentOS Linux release 8.4.2105
centos-release-upstream: Derived from Red Hat Enterprise Linux 8.4
os-release:
NAME="CentOS Linux"
VERSION="8"
ID="centos"
ID_LIKE="rhel fedora"
VERSION_ID="8"
PLATFORM_ID="platform:el8"
PRETTY_NAME="CentOS Linux 8"
ANSI_COLOR="0;31"
redhat-release: CentOS Linux release 8.4.2105
system-release: CentOS Linux release 8.4.2105
system-release-cpe: cpe:/o:centos:centos:8
```

uname -a:

```
Linux localhost.localdomain 4.18.0-305.3.1.el8.x86_64 #1 SMP Tue Jun 1 16:14:33 UTC
2021 x86_64 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

```
CVE-2018-12207 (iTLB Multihit): KVM: Mitigation: Split huge pages
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store
Bypass disabled via prctl and
seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs
barriers and __user pointer
```

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## Platform Notes (Continued)

CVE-2017-5715 (Spectre variant 2): sanitization  
Mitigation: Enhanced IBRS, IBPB:  
conditional, RSB filling  
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected  
CVE-2019-11135 (TSX Asynchronous Abort): Mitigation: TSX disabled

run-level 3 Aug 6 11:27

SPEC is set to: /home/cpu2017

```
Filesystem      Type  Size  Used Avail Use% Mounted on
/dev/mapper/cl-home xfs   372G   76G  296G  21% /home
```

```
From /sys/devices/virtual/dmi/id
Vendor:          Tyrone Systems
Product:         Tyrone Camarero DIT400TR-48RL
Product Family: empty
Serial:          empty
```

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:  
12x Samsung M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2400

BIOS:  
BIOS Vendor: American Megatrends Inc.  
BIOS Version: V8.104  
BIOS Date: 07/27/2021  
BIOS Revision: 5.14  
Firmware Revision: 6.1

(End of data from sysinfo program)

## Compiler Version Notes

```
=====
C          | 619.lbm_s(base, peak) 638.imagick_s(base, peak)
          | 644.nab_s(base)
-----
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
=====
```

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## Compiler Version Notes (Continued)

C | 644.nab\_s(peak)

-----  
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
-----

=====  
C | 619.lbm\_s(base, peak) 638.imagick\_s(base, peak)  
| 644.nab\_s(base)

-----  
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)  
64, Version 2021.1 Build 20201112\_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
-----

=====  
C | 644.nab\_s(peak)

-----  
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
-----

=====  
C++, C, Fortran | 607.cactuBSSN\_s(base, peak)

-----  
Intel(R) C++ Intel(R) 64 Compiler Classic for applications running on  
Intel(R) 64, Version 2021.1 Build 20201112\_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)  
64, Version 2021.1 Build 20201112\_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on  
Intel(R) 64, Version 2021.1 Build 20201112\_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.  
-----

=====  
Fortran | 603.bwaves\_s(base, peak) 649.fotonik3d\_s(base, peak)  
| 654.roms\_s(base, peak)

-----  
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on  
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## Compiler Version Notes (Continued)

```
=====
Fortran, C      | 621.wrf_s(base, peak) 627.cam4_s(base, peak)
                 | 628.pop2_s(base, peak)
=====
```

```
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
=====
```

## Base Compiler Invocation

C benchmarks:  
icc

Fortran benchmarks:  
ifort

Benchmarks using both Fortran and C:  
ifort icc

Benchmarks using Fortran, C, and C++:  
icpc icc ifort

## Base Portability Flags

```
603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64
```





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## Base Optimization Flags

C benchmarks:

```
-m64 -std=c11 -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP  
-mbranches-within-32B-boundaries
```

Fortran benchmarks:

```
-m64 -Wl,-z,muldefs -DSPEC_OPENMP -xCORE-AVX512 -ipo -O3  
-no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=4 -qopenmp -nostandard-realloc-lhs  
-mbranches-within-32B-boundaries -L/usr/local/je5.0.1-64/lib -ljemalloc
```

Benchmarks using both Fortran and C:

```
-m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp  
-DSPEC_OPENMP -mbranches-within-32B-boundaries -nostandard-realloc-lhs  
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

Benchmarks using Fortran, C, and C++:

```
-m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp  
-DSPEC_OPENMP -mbranches-within-32B-boundaries -nostandard-realloc-lhs  
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

## Peak Compiler Invocation

C benchmarks (except as noted below):

```
icc
```

```
644.nab_s: icx
```

Fortran benchmarks:

```
ifort
```

Benchmarks using both Fortran and C:

```
ifort icc
```

Benchmarks using Fortran, C, and C++:

```
icpc icc ifort
```



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## Peak Portability Flags

Same as Base Portability Flags

## Peak Optimization Flags

C benchmarks:

619.lbm\_s: basepeak = yes

638.imagick\_s: basepeak = yes

644.nab\_s: -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math  
-flto -mfpmath=sse -funroll-loops -fiopenmp  
-DSPEC\_OPENMP -qopt-mem-layout-trans=4  
-fimf-accuracy-bits=14:sqrt  
-mbranches-within-32B-boundaries  
-L/usr/local/je5.0.1-64/lib -ljemalloc

Fortran benchmarks:

603.bwaves\_s: -m64 -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)  
-DSPEC\_SUPPRESS\_OPENMP -DSPEC\_OPENMP -ipo -xCORE-AVX512  
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=4 -qopenmp -nostandard-realloc-lhs  
-mbranches-within-32B-boundaries  
-L/usr/local/je5.0.1-64/lib -ljemalloc

649.fotonik3d\_s: Same as 603.bwaves\_s

654.roms\_s: basepeak = yes

Benchmarks using both Fortran and C:

621.wrf\_s: -m64 -std=c11 -Wl,-z,muldefs -prof-gen(pass 1)  
-prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div  
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4  
-DSPEC\_SUPPRESS\_OPENMP -qopenmp -DSPEC\_OPENMP  
-mbranches-within-32B-boundaries -nostandard-realloc-lhs  
-L/usr/local/je5.0.1-64/lib -ljemalloc

627.cam4\_s: basepeak = yes

628.pop2\_s: basepeak = yes

(Continued on next page)



# SPEC CPU®2017 Floating Point Speed Result

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**Tyrone Systems**

(Test Sponsor: Netweb Pte Ltd)

**Tyrone Camarero DIT400TR-48RL**  
(2.10 GHz, Intel Xeon Silver 4216)

SPECspeed®2017\_fp\_base = 108

SPECspeed®2017\_fp\_peak = 111

**CPU2017 License:** 006042

**Test Sponsor:** Netweb Pte Ltd

**Tested by:** Tyrone Systems

**Test Date:** Aug-2021

**Hardware Availability:** Apr-2019

**Software Availability:** Jun-2021

## Peak Optimization Flags (Continued)

Benchmarks using Fortran, C, and C++:

607.cactuBSSN\_s: basepeak = yes

The flags files that were used to format this result can be browsed at

[http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64\\_revA.html](http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.html)

<http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revI.html>

You can also download the XML flags sources by saving the following links:

[http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64\\_revA.xml](http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml)

<http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revI.xml>

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