## SPEC CPU®2017 Floating Point Rate Result

### Tyrone Systems

(Test Sponsor: Netweb Pte Ltd)

**Tyrone Camarero DIT400TR-28RL**

(2.20 GHz, Intel Xeon Silver 4214)

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<table>
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<tr>
<th>Copies</th>
<th>SPECrate®2017_fp_base</th>
<th>SPECrate®2017_fp_peak</th>
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<td>503.bwaves_r</td>
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<td>508.namd_r</td>
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<tr>
<td>554.roms_r</td>
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</table>

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### Hardware

- **CPU Name:** Intel Xeon Silver 4214
- **Max MHz:** 3200
- **Nominal:** 2200
- **Enabled:** 24 cores, 2 chips, 2 threads/core
- **Orderable:** 1,2 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 16.5 MB I+D on chip per chip
- **Other:** None
- **Memory:** 384 GB (12 x 32 GB 2Rx4 PC4-2933P-R, running at 2400)
- **Storage:** 1 x 480 GB SATA SSD
- **Other:** None

### Software

- **OS:** CentOS Linux release 8.4.2105
  Kernel 4.18.0-305.3.1.el8.x86_64
- **Compiler:** C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux;
  Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux;
- **Firmware:** No
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 64-bit
- **Other:** jemalloc memory allocator V5.0.1
- **Power Management:** BIOS set to prefer performance at the cost of additional power usage.

---

**CPU2017 License:** 006042

**Test Sponsor:** Netweb Pte Ltd

**Test Date:** Aug-2021

**Hardware Availability:** Apr-2019

**Software Availability:** Jul-2021

---

**Tested by:** Tyrone Systems

**Test Date:** Aug-2021

**Hardware Availability:** Apr-2019

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**Test Sponsor:** Netweb Pte Ltd

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## Results Table

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**SPECrate®2017_fp_base = 150**

**SPECrate®2017_fp_peak = 151**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## Environment Variables Notes

Environment variables set by runcpu before the start of the run:

- **LD_LIBRARY_PATH** = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
- **MALLOC_CONF** = "retain:true"

## General Notes

Binaries compiled locally by Netweb
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:

```bash
sync; echo 3>/proc/sys/vm/drop_caches
drop_caches
```

runcpu command invoked through numactl i.e.:
Tyrone Systems  
(Test Sponsor: Netweb Pte Ltd)

Tyrone Camarero DIT400TR-28RL  
(2.20 GHz, Intel Xeon Silver 4214)

General Notes (Continued)

```bash
numactl --interleave=all runcpu <etc>
```

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.


Platform Notes

BIOS Settings:
Power Technology set to Custom
Power Performance Tuning set to BIOS Controls EPB
ENERGY_PERF_BIAS_CFG mode set to Performance
LLC Dead Line Alloc set to Disable

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16aca64d
running on spec Sat Aug  7 01:39:57 2021

SUT (System Under Test) info as seen by some common utilities. For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
```
model name : Intel(R) Xeon(R) Silver 4214 CPU @ 2.20GHz
  2 "physical id"s (chips)
  48 "processors"
 cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 12
  siblings : 24
  physical 0: cores 0 1 2 3 4 5 8 9 10 11 12 13
  physical 1: cores 0 1 2 3 4 5 8 9 10 11 12 13
```

From lscpu from util-linux 2.32.1:
```
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 48
On-line CPU(s) list: 0-47
Thread(s) per core: 2
```

(Continued on next page)
Platform Notes (Continued)

Core(s) per socket:  12
Socket(s):           2
NUMA node(s):        2
Vendor ID:           GenuineIntel
BIOS Vendor ID:      Intel(R) Corporation
CPU family:          6
Model:               85
Model name:          Intel(R) Xeon(R) Silver 4214 CPU @ 2.20GHz
BIOS Model name:     Intel(R) Xeon(R) Silver 4214 CPU @ 2.20GHz
Stepping:            7
CPU MHz:             2855.595
CPU max MHz:         3200.000
CPU min MHz:         1000.000
BogoMIPS:            4400.00
Virtualization:      VT-x
L1d cache:           32K
L1i cache:           32K
L2 cache:            1024K
L3 cache:            16896K
NUMA node0 CPU(s):   0-11,24-35
NUMA node1 CPU(s):   12-23,36-47
Flags:               fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
                       pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
                       lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
                       aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
                       xtrr pdcm pclid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
                       avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3
                       invpcid_single intel_pinn ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vmmi
                       flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erdms
                       invvpcid cid mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt
                       avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc
                       cqm_mbb_total cqm_mbb_local dtherm ida arat pln pts hwp hwp_act_window hwp_epp
                       hwp_pkg_req pkru ospke avx512_vnni md_clear flush_lld arch_capabilities

/proc/cpuinfo cache data
cache size : 16896 KB

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 2 nodes (0-1)
node 0 cpus:  0 1 2 3 4 5 6 7 8 9 10 11 24 25 26 27 28 29 30 31 32 33 34 35
node 0 size: 192108 MB
node 0 free: 178780 MB
node 1 cpus: 12 13 14 15 16 17 18 19 20 21 22 23 36 37 38 39 40 41 42 43 44 45 46 47
node 1 size: 193493 MB
node 1 free: 181951 MB
node distances:

(Continued on next page)
SPEC CPU®2017 Floating Point Rate Result

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero DIT400TR-28RL
(2.20 GHz, Intel Xeon Silver 4214)

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

SPECrace®2017_fp_base = 150
SPECrace®2017_fp_peak = 151

Platform Notes (Continued)

node   0   1
0:  10  21
1:  21  10

From /proc/meminfo
MemTotal:       394855532 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

/sbin/tuned-adm active
Current active profile: throughput-performance

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
centos-release: CentOS Linux release 8.4.2105
centos-release-upstream: Derived from Red Hat Enterprise Linux 8.4
os-release:
   NAME="CentOS Linux"
   VERSION="8"
   ID="centos"
   ID_LIKE="rhel fedora"
   VERSION_ID="8"
   PLATFORM_ID="platform:el8"
   PRETTY_NAME="CentOS Linux 8"
   ANSI_COLOR="0;31"
redhat-release: CentOS Linux release 8.4.2105
system-release: CentOS Linux release 8.4.2105
system-release-cpe: cpe:/o:centos:centos:8

uname -a:
   Linux spec 4.18.0-305.3.1.el8.x86_64 #1 SMP Tue Jun 1 16:14:33 UTC 2021 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit):
CVE-2018-3620 (L1 Terminal Fault):
Microarchitectural Data Sampling:
CVE-2017-5754 (Meltdown):
CVE-2018-3639 (Speculative Store Bypass):
CVE-2017-5753 (Spectre variant 1):

KVM: Mitigation: Split huge pages
Not affected
Not affected
Not affected
Mitigation: Speculative Store Bypass disabled via prctl and seccomp
Mitigation: usercopy/swapsgs barriers and __user pointer sanitization

(Continued on next page)
## SPEC CPU®2017 Floating Point Rate Result

**Tyrone Systems**  
(Test Sponsor: Netweb Pte Ltd)  
**Tyrone Camarero DIT400TR-28RL**  
(2.20 GHz, Intel Xeon Silver 4214)

<table>
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<tr>
<th>CPU2017 License:</th>
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<th>Test Date:</th>
<th>Aug-2021</th>
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<td>Apr-2019</td>
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<td>Jul-2021</td>
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</tbody>
</table>

### SPECrate®2017_fp_base = 150

### SPECrate®2017_fp_peak = 151

#### Platform Notes (Continued)

CVE-2017-5715 (Spectre variant 2):  
Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected

CVE-2019-11135 (TSX Asynchronous Abort):  
Mitigation: TSX disabled

run-level 3 Aug 6 16:55

SPEC is set to: /home/cpu2017

<table>
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<tr>
<th>Filesystem</th>
<th>Type</th>
<th>Size</th>
<th>Used</th>
<th>Avail</th>
<th>Use%</th>
<th>Mounted on</th>
</tr>
</thead>
<tbody>
<tr>
<td>/dev/mapper/cl-home</td>
<td>xfs</td>
<td>372G</td>
<td>193G</td>
<td>180G</td>
<td>52%</td>
<td>/home</td>
</tr>
</tbody>
</table>

From /sys/devices/virtual/dmi/id

- Vendor: Tyrone Systems
- Product: Tyrone Camarero DIT400TR-28RL
- Product Family: empty
- Serial: empty

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:  
12x Samsung M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2400

BIOS:  
- BIOS Vendor: American Megatrends Inc.
- BIOS Version: V8.104
- BIOS Date: 07/27/2021
- BIOS Revision: 5.14
- Firmware Revision: 6.1

(End of data from sysinfo program)

#### Compiler Version Notes

```plaintext
C                      |
| 519.lbm_r(base, peak) 538.imagick_r(base, peak)
| 544.nab_r(base, peak)

Intel(R) oneAPI DPC+/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113
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C++                    |
| 508.namd_r(base, peak) 510.parest_r(base, peak)
```

(Continued on next page)
Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero DIT400TR-28RL
(2.20 GHz, Intel Xeon Silver 4214)

SPECrater®2017_fp_base = 150
SPECrater®2017_fp_peak = 151

Compiler Version Notes (Continued)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
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Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

-----------------------------------------------------------------------------

C++, C | 511.povray_r(peak)

-----------------------------------------------------------------------------

Intel(R) C++ Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

-----------------------------------------------------------------------------

C++, C | 511.povray_r(base) 526.blender_r(base, peak)

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**Compiler Version Notes (Continued)**

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(Continued on next page)
**Compiler Version Notes (Continued)**

Fortran, C  |  521.wrf_r(peak)

=================================================================================================

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
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=================================================================================================

Fortran, C  |  521.wrf_r(base) 527.cam4_r(base, peak)

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Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
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=================================================================================================

**Base Compiler Invocation**

C benchmarks: icx

C++ benchmarks: icpx

Fortran benchmarks: ifort

Benchmarks using both Fortran and C: ifort icx

Benchmarks using both C and C++: icpx icx

Benchmarks using Fortran, C, and C++: icpx icx ifort
SPEC CPU®2017 Floating Point Rate Result

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero DIT400TR-28RL
(2.20 GHz, Intel Xeon Silver 4214)

SPECrater®2017_fp_base = 150
SPECrater®2017_fp_peak = 151

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

Test Date: Aug-2021
Hardware Availability: Apr-2019
Software Availability: Jul-2021

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-w -std=c11 -m64 -Wl,-z,muldefs -xcORE-AVX512 -Ofast -ffast-math
-fldt -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc -L/usr/local/je5.0.1-64/lib

C++ benchmarks:
-w -m64 -Wl,-z,muldefs -xcORE-AVX512 -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc -L/usr/local/je5.0.1-64/lib

Fortran benchmarks:
-w -m64 -Wl,-z,muldefs -xcORE-AVX512 -O3 -ipo -no-prec-div
-qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto
-mbranches-within-32B-boundaries -ljemalloc -L/usr/local/je5.0.1-64/lib

Benchmarks using both Fortran and C:
-w -m64 -std=c11 -Wl,-z,muldefs -xcORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-align array32byte -auto -ljemalloc -L/usr/local/je5.0.1-64/lib

Benchmarks using both C and C++:
-w -m64 -std=c11 -Wl,-z,muldefs -xcORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4

(Continued on next page)
**SPEC CPU®2017 Floating Point Rate Result**

Standard Performance Evaluation Corporation

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**Tyrone Systems**
(Test Sponsor: Netweb Pte Ltd)

**Tyrone Camarero DIT400TR-28RL**
(2.20 GHz, Intel Xeon Silver 4214)

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**SPECrate®2017_fp_base = 150**

**SPECrate®2017_fp_peak = 151**

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**Base Optimization Flags (Continued)**

Benchmarks using both C and C++ (continued):
-mbranches-within-32B-boundaries -ljemalloc -L/usr/local/je5.0.1-64/lib

Benchmarks using Fortran, C, and C++:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-fflto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-align array32byte -auto -ljemalloc -L/usr/local/je5.0.1-64/lib

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**Peak Compiler Invocation**

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
521.wrf_r:ifort icc
527.cam4_r:ifort icx

Benchmarks using both C and C++:
511.povray_r:icpc icc
526.blender_r:icpx icx

Benchmarks using Fortran, C, and C++:
icpx icx ifort

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**Peak Portability Flags**

Same as Base Portability Flags
SPEC CPU®2017 Floating Point Rate Result

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero DIT400TR-28RL
(2.20 GHz, Intel Xeon Silver 4214)

SPECrate®2017_fp_base = 150
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CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Test Date: Aug-2021
Tested by: Tyrone Systems
Hardware Availability: Apr-2019
Software Availability: Jul-2021

Peak Optimization Flags

C benchmarks:

519.lbm_r: basepeak = yes

538.imagick_r: basepeak = yes

544.nab_r: -w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -flto
-Ofast -qopt-mem-layout-trans=4
-fimf-accuracy-bits=14:sqrt
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/je5.0.1-64/lib

C++ benchmarks:

508.namd_r: basepeak = yes

510.parest_r: -w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-ljemalloc -L/usr/local/je5.0.1-64/lib

Fortran benchmarks:

503.bwaves_r: -w -m64 -Wl,-z,muldeps -xCORE-AVX512 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs
-align array32byte -auto -mbranches-within-32B-boundaries
-ljemalloc -L/usr/local/je5.0.1-64/lib

549.fotonik3d_r: basepeak = yes

554.roms_r: Same as 503.bwaves_r

Benchmarks using both Fortran and C:

521.wrf_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3
-ipo -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-nostandard-realloc-lhs -align array32byte -auto
-L/usr/local/je5.0.1-64/lib -ljemalloc

527.cam4_r: basepeak = yes

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Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero DIT400TR-28RL
(2.20 GHz, Intel Xeon Silver 4214)

SPECrate®2017_fp_base = 150
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CPU2017 License: 006042
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Tested by: Tyrone Systems

Test Date: Aug-2021
Hardware Availability: Apr-2019
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Peak Optimization Flags (Continued)

Benchmarks using both C and C++:

511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3
-ipo -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/usr/local/je5.0.1-64/lib -ljemalloc

526.blender_r: basepeak = yes

Benchmarks using Fortran, C, and C++:

507.cactuBSSN_r: basepeak = yes

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revI.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revI.xml