**SPEC CPU®2017 Integer Speed Result**

**Tyrone Systems**  
(Test Sponsor: Netweb Pte Ltd)

**Tyrone Camarero SDI100A2G-210**  
(2.60 GHz, Intel Xeon Gold 6348)

<table>
<thead>
<tr>
<th>Software</th>
<th><strong>SPECspeed®2017_int_base = 11.6</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td><strong>SPECspeed®2017_int_peak = 11.9</strong></td>
</tr>
</tbody>
</table>

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<table>
<thead>
<tr>
<th>Time (s)</th>
<th>SPECspeed®2017_int_base</th>
<th>SPECspeed®2017_int_peak</th>
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<tbody>
<tr>
<td>112</td>
<td>7.24</td>
<td>11.9</td>
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<td>112</td>
<td>8.30</td>
<td>11.6</td>
</tr>
<tr>
<td>112</td>
<td>9.46</td>
<td></td>
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<tr>
<td>112</td>
<td>13.5</td>
<td></td>
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<tr>
<td>112</td>
<td>16.9</td>
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<td>112</td>
<td>19.0</td>
<td></td>
</tr>
<tr>
<td>112</td>
<td>24.1</td>
<td></td>
</tr>
</tbody>
</table>

---

**Hardware**

- **CPU Name**: Intel Xeon Gold 6348  
- **Max MHz**: 3500  
- **Nominal**: 2600  
- **Enabled**: 56 cores, 2 chips, 2 threads/core  
- **Orderable**: 1.2 Chips  
- **Cache L1**: 32 KB I + 48 KB D on chip per core  
- **L2**: 1.25 MB I+D on chip per core  
- **L3**: 42 MB I+D on chip per chip  
- **Other**: None  
- **Memory**: 256 GB (7 x 16 GB 1Rx4 PC4-3200AA-R; 9 x 16 GB 2Rx8 PC4-3200AA-R)  
- **Storage**: 1 x 256 GB SATA SSD  
- **Other**: None

---

**Software**

- **OS**: CentOS Linux release 8.4.2105  
- **Kernel**: 4.18.0-305.3.1.el8.x86_64  
- **Compiler**: C/C++, Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux; Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux; C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20210112 for Linux;  
- **Parallel**: Yes  
- **Firmware**: Version 1.1 released Apr-2021  
- **File System**: xfs  
- **System State**: Run level 3 (multi-user)  
- **Base Pointers**: 64-bit  
- **Peak Pointers**: 64-bit  
- **Other**: jemalloc memory allocator V5.0.1  
- **Power Management**: BIOS set to prefer performance at the cost of additional power usage.
### Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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<tr>
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<td>112</td>
<td>245</td>
<td>7.24</td>
<td>247</td>
<td>7.19</td>
<td>245</td>
<td>7.24</td>
<td>112</td>
<td>211</td>
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<td>212</td>
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<tr>
<td>602.gcc_s</td>
<td>112</td>
<td>361</td>
<td>11.0</td>
<td>364</td>
<td>10.9</td>
<td>368</td>
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<td>11.4</td>
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<td>605.mcf_s</td>
<td>112</td>
<td>323</td>
<td>20.3</td>
<td>329</td>
<td>19.8</td>
<td>329</td>
<td>19.8</td>
<td>112</td>
<td>233</td>
<td>20.3</td>
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<td>239</td>
<td>19.8</td>
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<tr>
<td>620.omnetpp_s</td>
<td>112</td>
<td>175</td>
<td>9.34</td>
<td>172</td>
<td>9.46</td>
<td>171</td>
<td>9.54</td>
<td>112</td>
<td>175</td>
<td>9.34</td>
<td></td>
<td>172</td>
<td>9.46</td>
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<td>623.xalanchmk_s</td>
<td>112</td>
<td>105</td>
<td>13.5</td>
<td>104</td>
<td>13.6</td>
<td>105</td>
<td>13.5</td>
<td>112</td>
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<tr>
<td>625.x264_s</td>
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<td>104</td>
<td>16.9</td>
<td>105</td>
<td>16.9</td>
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<td></td>
<td>99.7</td>
<td>17.7</td>
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<td>5.95</td>
<td>241</td>
<td>5.95</td>
<td>241</td>
<td>5.96</td>
<td>112</td>
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<td>641.leela_s</td>
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<td>648.exchange2_s</td>
<td>112</td>
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<td>155</td>
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<td>155</td>
<td>19.0</td>
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<td>154</td>
<td>19.1</td>
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<td>155</td>
<td>19.0</td>
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<tr>
<td>657.xz_s</td>
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<td>24.1</td>
<td>258</td>
<td>24.0</td>
<td>256</td>
<td>24.1</td>
<td>112</td>
<td>257</td>
<td>24.1</td>
<td></td>
<td>258</td>
<td>24.0</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:
- KMP_AFFINITY = "granularity=fine,scatter"
- LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
- MALLOC_CONF = "retain:true"
- OMP_STACKSIZE = "192M"

### General Notes

Binaries compiled locally by Netweb
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
```
sync; echo 3> /proc/sys/vm/drop_caches
```

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

(Continued on next page)
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SPECspeed®2017_int_peak = 11.9

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

General Notes (Continued)

Platform Notes

BIOS Settings:
Power Technology set to Custom
Power Performance Tuning set to BIOS Controls EPB
ENERGY_PERF_BIAS_CFG mode set to Performance
LLC Dead Line Alloc set to Disable

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16aca61c64d
running on localhost.localdomain Wed Jul 28 13:39:40 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6348 CPU @ 2.60GHz
 2 "physical id"s (chips)
112 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
eccerts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 28
siblings : 56
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
25 26 27
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
25 26 27

From lscpu from util-linux 2.32.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 112
On-line CPU(s) list: 0-111
Thread(s) per core: 2
Core(s) per socket: 28
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
BIOS Vendor ID: Intel(R) Corporation
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Gold 6348 CPU @ 2.60GHz

(Continued on next page)
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CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

Platform Notes (Continued)

BIOS Model name: Intel(R) Xeon(R) Gold 6348 CPU @ 2.60GHz
Stepping: 6
CPU MHz: 2070.569
CPU max MHz: 3500.0000
CPU min MHz: 800.0000
BogoMIPS: 5200.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 43008K
NUMA node0 CPU(s): 0-13, 56-69
NUMA node1 CPU(s): 14-27, 70-83
NUMA node2 CPU(s): 28-41, 84-97
NUMA node3 CPU(s): 42-55, 98-111
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpica smx swx ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmprefetch pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abm 3nowprefetch cpuid_fault epb cat_l3 invpcid_single
intel_puin ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnu1 flexpriority ept
vpid ept_ad fsnode base tsc_adjust bmi1 hle avx2 smep bmi2 ertms invpcid çqm rdt_a
avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha ni
avx512bw avx512vl xsaveopt xsavecv xgetbv1 xsavec çqm_llc çqm_occup_llc çqm_mbdtotal
çqm_mbdt_local split_lock_detect wboinvd dtherm ida arat pln pts avx512vbmi umip pku
ospe avx512_vbmi2 gfi nae vpcmtdq avx512_vni avx512_bitalg tme
avx512_vpopcntdq la57 rdpid fsrmd md_clear pconfig flush_1ld arch_capabilities

/proc/cpuinfo cache data
cache size : 43008 KB

From numacl --hardware
WARNING: a numacl 'node' might or might not correspond to a physical chip.
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 56 57 58 59 60 61 62 63 64 65 66 67 68 69
node 0 size: 64095 MB
node 0 free: 43255 MB
node 1 cpus: 14 15 16 17 18 19 20 21 22 23 24 25 26 27 70 71 72 73 74 75 76 77 78 79 80
81 82 83
node 1 size: 64468 MB
node 1 free: 47031 MB
node 2 cpus: 28 29 30 31 32 33 34 35 36 37 38 39 40 41 84 85 86 87 88 89 90 91 92 93 94
95 96 97
node 2 size: 64505 MB
node 2 free: 47060 MB
node 3 cpus: 42 43 44 45 46 47 48 49 50 51 52 53 54 55 98 99 100 101 102 103 104 105

(Continued on next page)
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Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

Platform Notes (Continued)

106 107 108 109 110 111	node 3 size: 64503 MB	node 3 free: 47140 MB	node distances:
node 0 1 2 3
0: 10 11 20 20
1: 11 10 20 20
2: 20 20 10 11
3: 20 20 11 10

From /proc/meminfo
MemTotal: 263755296 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/sbin/tuned-adm active
Current active profile: throughput-performance

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
centos-release: CentOS Linux release 8.4.2105
centos-release-upstream: Derived from Red Hat Enterprise Linux 8.4
os-release:
NAME="CentOS Linux"
VERSION="8"
ID="centos"
ID_LIKE="rhel fedora"
VERSION_ID="8"
PLATFORM_ID="platform:el8"
PRETTY_NAME="CentOS Linux 8"
ANSI_COLOR="0;31"
redhat-release: CentOS Linux release 8.4.2105
system-release: CentOS Linux release 8.4.2105
system-release-cpe: cpe:/o:centos:centos:8

uname -a:
Linux localhost.localdomain 4.18.0-305.3.1.el8.x86_64 #1 SMP Tue Jun 1 16:14:33 UTC 2021 x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected

(Continued on next page)
**Platform Notes (Continued)**

CVE-2018-3639 (Speculative Store Bypass):
Mitigation: Speculative Store Bypass disabled via prctl and seccomp

CVE-2017-5753 (Spectre variant 1):
Mitigation: usercopy/swapgs barriers and __user pointer sanitization

CVE-2017-5715 (Spectre variant 2):
Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Jul 27 08:14

SPEC is set to: /home/cpu2017

```
<table>
<thead>
<tr>
<th>Filesystem</th>
<th>Type</th>
<th>Size</th>
<th>Used</th>
<th>Avail</th>
<th>Use%</th>
<th>Mounted on</th>
</tr>
</thead>
<tbody>
<tr>
<td>/dev/mapper/cl-home</td>
<td>xfs</td>
<td>163G</td>
<td>71G</td>
<td>92G</td>
<td>44%</td>
<td>/home</td>
</tr>
</tbody>
</table>
```

From /sys/devices/virtual/dmi/id

```
Vendor:         Tyrone Systems
Product:        Tyrone Camarero SDI100A2G-210
Product Family: SMC X12
Serial:         123456789
```

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
- 7x Samsung M393A2K40DB3-CWE 16 GB 1 rank 3200
- 9x Samsung M393A2K43DB3-CWE 16 GB 2 rank 3200

BIOS:
- BIOS Vendor: American Megatrends International, LLC.
- BIOS Version: 1.1
- BIOS Date: 04/21/2021
- BIOS Revision: 5.22

(End of data from sysinfo program)

**Compiler Version Notes**

```
C       | 600.perlbench_s(peak)
```

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000

(Continued on next page)
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<td>SPECspeed®2017_int_peak = 11.9</td>
<td>Hardware Availability: Apr-2021</td>
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</table>

**CPU2017 License:** 006042  
**Test Sponsor:** Netweb Pte Ltd  
**Tested by:** Tyrone Systems

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<tr>
<th>Test Date: Jul-2021</th>
<th>Hardware Availability: Apr-2021</th>
</tr>
</thead>
<tbody>
<tr>
<td>Software Availability: Jun-2021</td>
<td></td>
</tr>
</tbody>
</table>

**Compiler Version Notes (Continued)**

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

```
------------------------------------------------------------------------------
|                      | 600.perlbench_s(base) 602.gcc_s(base, peak) 605.mcf_s(base, peak) |
|                      | 625.x264_s(base, peak) 657.xz_s(base, peak) |
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
|                      | 600.perlbench_s(peak) |
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)  
64, Version 2021.1 Build 20201112_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
|                      | 600.perlbench_s(base) 602.gcc_s(base, peak) 605.mcf_s(base, peak) |
|                      | 625.x264_s(base, peak) 657.xz_s(base, peak) |
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
|                      | 620.omnetpp_s(base, peak) 623.xalancbmk_s(base, peak) |
|                      | 631.deepsjeng_s(base, peak) 641.leela_s(base, peak) |
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
|                      | 648.exchange2_s(base, peak) |
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on  
Intel(R) 64, Version 2021.1 Build 20201112_000000  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
```
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Hardware Availability: Apr-2021
Software Availability: Jun-2021

Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Base Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-DSPEC_OPENMP -std=c11 -m64 -fopenmp -Wl,-z,muldefs -xCORE-AVX512
-O3 -ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:
-DSPEC_OPENMP -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin/
-lqkmalloc

Fortran benchmarks:
-m64 -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte
-mbranches-within-32B-boundaries
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</table>

**Peak Compiler Invocation**

C benchmarks (except as noted below):
- icx
- 600.perlbench_s: icc

C++ benchmarks:
- icpx

Fortran benchmarks:
- ifort

**Peak Portability Flags**

Same as Base Portability Flags

**Peak Optimization Flags**

C benchmarks:
- 600.perlbench_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4 -fno-strict-overflow -mbranches-within-32B-boundaries -L/usr/local/je5.0.1-64/lib -ljemalloc
- 602.gcc_s: -m64 -std=c11 -Wl,-z,muldefs -fprofile-generate(pass 1) -fprofile-use=default.profd(pass 2) -xCORE-AVX512 -flio -Ofast(pass 1) -O3 -ffast-math -qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries -L/usr/local/je5.0.1-64/lib -ljemalloc
- 605.mcf_s: basepeak = yes
- 625.x264_s: -DSPEC_OPENMP -fiopenmp -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -flio -O3 -ffast-math -qopt-mem-layout-trans=4 -fno-alias -mbranches-within-32B-boundaries -L/usr/local/je5.0.1-64/lib -ljemalloc
- 657.xz_s: basepeak = yes

(Continued on next page)
### SPEC CPU®2017 Integer Speed Result

**Tyrone Systems**  
(Test Sponsor: Netweb Pte Ltd)  
Tyrone Camarero SDI100A2G-210  
(2.60 GHz,Intel Xeon Gold 6348)

**SPECspeed®2017_int_base = 11.6**  
**SPECspeed®2017_int_peak = 11.9**

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**Peak Optimization Flags (Continued)**

C++ benchmarks:

- 620.omnetpp_s: basepeak = yes
- 623.xalancbmk_s: basepeak = yes
- 631.deepsjeng_s: basepeak = yes
- 641.leela_s: basepeak = yes

Fortran benchmarks:

- 648.exchange2_s: basepeak = yes

The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links:

- [http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revI.xml](http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revI.xml)

### Notes

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- For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.
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