Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6342, 2.80GHz)

SPECspeed\textsuperscript{®}2017\textsuperscript{-fp\_peak} = 197
SPECspeed\textsuperscript{®}2017\textsuperscript{-fp\_base} = 196

**CPU2017 License:** 9019
**Test Sponsor:** Cisco Systems
**Tested by:** Cisco Systems
**Test Date:** Aug-2021
**Hardware Availability:** Apr-2021
**Software Availability:** Dec-2020

<table>
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<tr>
<th>Threads</th>
<th>603.bwaves.s</th>
<th>607.cactuBSSN.s</th>
<th>619.ibm.s</th>
<th>621.wrf.s</th>
<th>627.cam4.s</th>
<th>628.pop2.s</th>
<th>638.imagick.s</th>
<th>644.nab.s</th>
<th>649.fotonik3d.s</th>
<th>654.roms.s</th>
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<tr>
<td>630-660</td>
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</tr>
</tbody>
</table>

**SPECspeed\textsuperscript{®}2017\textsuperscript{-fp\_peak} (197)**

**SPECspeed\textsuperscript{®}2017\textsuperscript{-fp\_base} (196)**

### Hardware

- **CPU Name:** Intel Xeon Gold 6342
- **Max MHz:** 3500
- **Nominal:** 2800
- **Enabled:** 48 cores, 2 chips
- **Orderable:** 1.2 Chips
- **Cache L1:** 32 KB I + 48 KB D on chip per core
- **L2:** 1.25 MB I+D on chip per core
- **L3:** 36 MB I+D on chip per chip
- **Memory:** 1 TB (32 x 32 GB 2Rx4 PC4-3200V-R)
- **Storage:** 1 x 300 GB 15K SAS HDD
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 15 SP2 5.3.18-22-default
- **Compiler:** C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux;
  Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux;
  C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux
- **Parallel:** Yes
- **Firmware:** Version 4.2.1c released Jul-2021
- **File System:** btrfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 64-bit
- **Other:** jemalloc memory allocator V5.0.1
- **Power Management:** BIOS and OS set to prefer performance at the cost of additional power usage
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6342, 2.80GHz)

SPECspeed®2017_fp_base = 196
SPECspeed®2017_fp_peak = 197

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
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<td>603.bwaves_s</td>
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<td>683</td>
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<td>628.pop2_s</td>
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<td>649.fotonik3d_s</td>
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<td>67.8</td>
<td>232</td>
<td>67.3</td>
<td>234</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOC_CONF = "retain:true"
OMP_STACKSIZE = "192M"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM memory using Redhat Enterprise Linux 8.0
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6342, 2.80GHz)

Test Sponsor: Cisco Systems
Tested by: Cisco Systems

General Notes (Continued)


Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
UPI Link Enablement set to 1
UPI Power Management set to Enabled
Sub NUMA Clustering set to Disabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDDC Sparing set to Disabled
Patrol Scrub set to Disabled
Enhanced CPU performance set to Auto
Energy Efficient Turbo set to Enabled
Processor C6 Report set to Enabled
Processor C1E set to Enabled
Intel HyperThreading Technology set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acaf64d
running on localhost Tue Aug  3 10:35:20 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6342 CPU @ 2.80GHz
  2  "physical id"s (chips)
  48 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 24
siblings : 24
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23

From lscpu from util-linux 2.33.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 48
On-line CPU(s) list: 0-47

(Continued on next page)
**Platform Notes (Continued)**

- Thread(s) per core: 1
- Core(s) per socket: 24
- Socket(s): 2
- NUMA node(s): 2
- Vendor ID: GenuineIntel
- CPU family: 6
- Model: 106
- Model name: Intel(R) Xeon(R) Gold 6342 CPU @ 2.80GHz
- Stepping: 6
- CPU MHz: 3316.366
- CPU max MHz: 3500.0000
- CPU min MHz: 800.0000
- BogoMIPS: 5600.00
- Virtualization: VT-x
- L1d cache: 48K
- L1i cache: 32K
- L2 cache: 1280K
- L3 cache: 36864K
- NUMA node0 CPU(s): 0-23
- NUMA node1 CPU(s): 24-47
- Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3nowprefetch cpuid_fault epb cat_13 invpcid_single ssbd mba ibrs stibpibri enhanced tpr_shadow vmi flexpriority ept vpid ept_ad fsgsbase tsc_adjust bm1 hle avx2 smep bmi2 erms invpcid rtm cmp rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha_ni avx512bw avx512vl xsaveopt xsaveopt xsavec xsavec xsave xsavec cmqm llc cmqm_mbmlocal wbnoinvd dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req avx512vmbi umip pku ospke avx512_vmbi2 gfnl vaes vpmulqdqq avx512_vnni avx512_bitalg tme avx512_vpopcntdq ls57 rdpid md_clear pconfig flush_l1d arch_capabilities

From numactl --hardware
Warning: a numactl 'node' might or might not correspond to a physical chip.

- available: 2 nodes (0-1)
- node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
- node 0 size: 515649 MB
- node 0 free: 513877 MB
- node 1 cpus: 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47
- node 1 size: 516086 MB
- node 1 free: 509199 MB

(Continued on next page)
## Platform Notes (Continued)

- node distances:
  - node 0 1
  - 0: 10 20
  - 1: 20 10

From `/proc/meminfo`
- MemTotal: 1056498052 kB
- HugePages_Total: 0
- Hugepagesize: 2048 kB

From `/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor`
- Has performance

From `/etc/*release* /etc/*version*`
- `os-release`:
  - NAME="SLES"
  - VERSION="15-SP2"
  - VERSION_ID="15.2"
  - PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
  - ID="sles"
  - ID_LIKE="suse"
  - ANSI_COLOR="0;32"
  - CPE_NAME="cpe:/o:suse:sles:15:sp2"

**uname -a:**
- Linux localhost 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
- x86_64 GNU/Linux

Kernel self-reported vulnerability status:

- CVE-2018-12207 (iTLB Multihit):
  - Not affected
- CVE-2018-3620 (L1 Terminal Fault):
  - Not affected
- Microarchitectural Data Sampling:
  - Not affected
- CVE-2017-5754 (Meltdown):
  - Not affected
- CVE-2018-3639 (Speculative Store Bypass):
  - Mitigation: Speculative Store Bypass disabled via prctl and seccomp
- CVE-2017-5753 (Spectre variant 1):
  - Mitigation: usercopy/swapsgs barriers and __user pointer sanitization
- CVE-2017-5715 (Spectre variant 2):
  - Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
- CVE-2020-0543 (Special Register Buffer Data Sampling):
  - Not affected
- CVE-2019-11135 (TSX Asynchronous Abort):
  - Not affected

run-level 3 Aug 3 06:28

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6342, 2.80GHz)

SPEC CPU®2017 Floating Point Speed Result
Copyright 2017-2021 Standard Performance Evaluation Corporation

SPECspeed®2017_fp_base = 196
SPECspeed®2017_fp_peak = 197

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Platform Notes (Continued)

SPEC is set to: /home/cpu2017
Filesysten Type Size Used Avail Use% Mounted on
/dev/sda2 btrfs 222G 37G 184G 17% /home

From /sys/devices/virtual/dmi/id
Vendor: Cisco Systems Inc
Product: UCSC-C220-M6S
Serial: WZP24430ADF

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
32x 0xCE00 M393A4K40DB3-CWE 32 GB 2 rank 3200

BIOS:
BIOS Vendor: Cisco Systems, Inc.
BIOS Version: C220M6.4.2.1.c.1.0701210708
BIOS Date: 07/01/2021
BIOS Revision: 5.22

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C               | 619.lbm_s(base, peak) 638.imagick_s(base, peak)
| 644.nab_s(base)
==============================================================================

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================

==============================================================================
C               | 644.nab_s(peak)
==============================================================================

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================

==============================================================================
C               | 619.lbm_s(base, peak) 638.imagick_s(base, peak)
| 644.nab_s(base)
(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6342, 2.80GHz)

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<tr>
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<tr>
<td>SPECspeed®2017_fp_base</td>
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Aug-2021
Tested by: Cisco Systems
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Compiler Version Notes (Continued)

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
C               | 644.nab_s(peak)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
C++, C, Fortran | 607.cactuBSSN_s(base, peak)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
Fortran         | 603.bwaves_s(base, peak) 649.fotonik3d_s(base, peak)
| 654.roms_s(base, peak)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
Fortran, C      | 621.wrf_s(base, peak) 627.cam4_s(base, peak)
| 628.pop2_s(base, peak)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

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### Compiler Version Notes (Continued)

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#### Base Compiler Invocation

C benchmarks:

```
icc
```

Fortran benchmarks:

```
ifort
```

Benchmarks using both Fortran and C:

```
ifort icc
```

Benchmarks using Fortran, C, and C++:

```
icpc icc ifort
```

---

#### Base Portability Flags

```  
603.bwaves_s: -DSPEC_LP64  
607.cactuBSSN_s: -DSPEC_LP64  
619.lbm_s: -DSPEC_LP64  
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian  
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG  
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian  
-assume byterecl  
638.imagick_s: -DSPEC_LP64  
644.nab_s: -DSPEC_LP64  
649.fotonik3d_s: -DSPEC_LP64  
654.roms_s: -DSPEC_LP64
```

---

#### Base Optimization Flags

C benchmarks:

```  
-m64 -std=c11 -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP  
-mbranches-within-32B-boundaries
```

Fortran benchmarks:

```  
-m64 -Wl,-z,muldefs -DSPEC_OPENMP -xCORE-AVX2 -ipo -O3 -no-prec-div  
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp  
-nostandard-realloc-lhs -mbranches-within-32B-boundaries
```

(Continued on next page)
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
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Tested by: Cisco Systems
Hardware Availability: Apr-2021
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Base Optimization Flags (Continued)

Fortran benchmarks (continued):
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Benchmarks using both Fortran and C:
-m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX2 -ipo -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-DSPEC_OPENMP -mbranches-within-32B-boundaries -nostandard-realloc-lhs
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Benchmarks using Fortran, C, and C++:
-m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX2 -ipo -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-DSPEC_OPENMP -mbranches-within-32B-boundaries -nostandard-realloc-lhs
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Peak Compiler Invocation

C benchmarks (except as noted below):
icc
644.nab_s: icx

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6342, 2.80GHz)

SPECspeed®2017_fp_base = 196
SPECspeed®2017_fp_peak = 197

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Aug-2021
Tested by: Cisco Systems
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Peak Optimization Flags (Continued)

619.lbm_s: basepeak = yes

638.imagick_s: basepeak = yes

644.nab_s: -m64 -Wl,-z,muldefs -xCORE-AVX2 -Ofast -ffast-math
-fito -mfpmath=sse -funroll-loops -fiopenmp
-DSPEC_OPENMP -qopt-mem-layout-trans=4
-fimf-accuracy-bits=14:sqrt
-mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Fortran benchmarks:

603.bwaves_s: -m64 -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)
-DSPEC_SUPPRESS_OPENMP -DSPEC_OPENMP -ipo -xCORE-AVX2
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -qopenmp -nostandard-realloc-lhs
-mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

649.fotonik3d_s: Same as 603.bwaves_s

654.roms_s: basepeak = yes

Benchmarks using both Fortran and C:

621.wrf_s: -m64 -std=c11 -Wl,-z,muldefs -prof-gen(pass 1)
-prof-use(pass 2) -ipo -xCORE-AVX2 -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

627.cam4_s: basepeak = yes

628.pop2_s: basepeak = yes

Benchmarks using Fortran, C, and C++:

607.cactuBSSN_s: basepeak = yes

The flags files that were used to format this result can be browsed at
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6342, 2.80GHz)

<table>
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<tr>
<th>SPECspeed®2017_fp_base</th>
<th>SPECspeed®2017_fp_peak</th>
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<td>197</td>
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CPU2017 License: 9019
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Software Availability: Dec-2020

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml

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