Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Silver 4314, 2.40GHz)

<table>
<thead>
<tr>
<th>SPEC CPU®2017 Integer Speed Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU2017 License: 9019</td>
</tr>
<tr>
<td>Test Sponsor: Cisco Systems</td>
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<td>SPECspeed®2017_int_base = 11.1</td>
</tr>
<tr>
<td>SPECspeed®2017_int_peak = 11.4</td>
</tr>
</tbody>
</table>

| Threads | 0 | 1.00 | 2.00 | 3.00 | 4.00 | 5.00 | 6.00 | 7.00 | 8.00 | 9.00 | 10.0 | 11.0 | 12.0 | 13.0 | 14.0 | 15.0 | 16.0 | 17.0 | 18.0 | 19.0 | 20.0 | 21.0 | 22.0 |
|---------|---|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|      |
| 600.perlbench_s 32 | 6.91 | 7.53 | 10.4 | 10.7 |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |
| 602.gcc_s 32       | 5.74 | 6.91 | 10.4 | 10.7 |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |
| 605.mcf_s 32       | 4.75 | 5.74 | 10.4 | 10.7 |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |
| 631.deepsjeng_s 32 | 18.7 | 19.0 | 19.0 | 19.0 | 19.0  | 19.0  | 19.0  | 19.0 | 19.0 | 19.0 | 19.0 | 19.0 | 19.0 | 19.0 | 19.0 | 19.0 | 19.0 | 19.0 | 19.0 | 19.0 | 19.0 | 19.0 | 19.0 |
| 641.leela_s 32     | 13.0 | 14.0 | 15.0 | 16.0 | 17.0  | 18.0  | 19.0  | 20.0 | 21.0 | 22.0 | 23.0 | 24.0 | 25.0 | 26.0 | 27.0 | 28.0 | 29.0 | 30.0 | 31.0 | 32.0 | 33.0 | 34.0 | 35.0 |
| 648.exchange2_s 32 | 13.0 | 14.0 | 15.0 | 16.0 | 17.0  | 18.0  | 19.0  | 20.0 | 21.0 | 22.0 | 23.0 | 24.0 | 25.0 | 26.0 | 27.0 | 28.0 | 29.0 | 30.0 | 31.0 | 32.0 | 33.0 | 34.0 | 35.0 |
| 657.xz_s 32        | 13.0 | 14.0 | 15.0 | 16.0 | 17.0  | 18.0  | 19.0  | 20.0 | 21.0 | 22.0 | 23.0 | 24.0 | 25.0 | 26.0 | 27.0 | 28.0 | 29.0 | 30.0 | 31.0 | 32.0 | 33.0 | 34.0 | 35.0 |

**Hardware**
- CPU Name: Intel Xeon Silver 4314
- Max MHz: 3400
- Nominal: 2400
- Enabled: 32 cores, 2 chips
- Orderable: 1.2 Chips
- Cache L1: 32 KB I + 48 KB D on chip per core
- Cache L2: 1.25 MB I+D on chip per core
- Cache L3: 24 MB I+D on chip per chip
- Other: None
- Memory: 1 TB (32 x 32 GB 2Rx4 PC4-3200V-R, running at 2666)
- Storage: 1 x 300 GB 15K SAS HDD
- Other: None

**Software**
- OS: SUSE Linux Enterprise Server 15 SP2 5.3.18-22-default
- Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux; Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux; C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux
- Parallel: Yes
- Firmware: Version 4.2.1c released Jul-2021
- File System: btrfs
- System State: Run level 3 (multi-user)
- Base Pointers: 64-bit
- Peak Pointers: 64-bit
- Other: jemalloc memory allocator V5.0.1
- Power Management: BIOS and OS set to prefer performance at the cost of additional power usage
### Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
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<th>Ratio</th>
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<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>32</td>
<td>255</td>
<td>6.95</td>
<td>257</td>
<td>6.91</td>
<td>259</td>
<td>6.84</td>
<td>32</td>
<td>223</td>
<td>7.95</td>
<td>224</td>
<td>7.93</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>32</td>
<td>383</td>
<td>10.4</td>
<td>384</td>
<td>10.4</td>
<td>387</td>
<td>10.3</td>
<td>32</td>
<td>372</td>
<td>10.7</td>
<td>373</td>
<td>10.7</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>32</td>
<td>252</td>
<td>18.7</td>
<td>252</td>
<td>18.7</td>
<td>250</td>
<td>18.9</td>
<td>32</td>
<td>252</td>
<td>18.7</td>
<td>252</td>
<td>18.7</td>
<td>250</td>
<td>18.9</td>
<td></td>
<td></td>
</tr>
<tr>
<td>625.x264_s</td>
<td>32</td>
<td>109</td>
<td>16.2</td>
<td>109</td>
<td>16.2</td>
<td>109</td>
<td>16.2</td>
<td>32</td>
<td>104</td>
<td>16.9</td>
<td>104</td>
<td>16.9</td>
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<td></td>
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<td>631.deepsjeng_s</td>
<td>32</td>
<td>250</td>
<td>5.74</td>
<td>249</td>
<td>5.74</td>
<td>249</td>
<td>5.75</td>
<td>32</td>
<td>250</td>
<td>5.74</td>
<td>249</td>
<td>5.74</td>
<td>249</td>
<td>5.75</td>
<td></td>
<td></td>
</tr>
<tr>
<td>641.leea_s</td>
<td>32</td>
<td>359</td>
<td>4.75</td>
<td>359</td>
<td>4.75</td>
<td>359</td>
<td>4.75</td>
<td>32</td>
<td>359</td>
<td>4.75</td>
<td>359</td>
<td>4.75</td>
<td>359</td>
<td>4.75</td>
<td></td>
<td></td>
</tr>
<tr>
<td>648.exchange2_s</td>
<td>32</td>
<td>156</td>
<td>18.9</td>
<td>156</td>
<td>18.8</td>
<td>156</td>
<td>18.8</td>
<td>32</td>
<td>156</td>
<td>18.9</td>
<td>156</td>
<td>18.8</td>
<td>156</td>
<td>18.8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>657.xz_s</td>
<td>32</td>
<td>290</td>
<td>21.3</td>
<td>290</td>
<td>21.3</td>
<td>290</td>
<td>21.3</td>
<td>32</td>
<td>290</td>
<td>21.3</td>
<td>290</td>
<td>21.3</td>
<td>290</td>
<td>21.3</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:
- **KMP_AFFINITY** = "granularity=fine,scatter"
- **LD_LIBRARY_PATH** = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
- **MALLOC_CONF** = "retain:true"
- **OMP_STACKSIZE** = "192M"

### General Notes

Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM
Memory using Redhat Enterprise Linux 8.0
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesyste page cache synced and cleared with:
sync; echo 3 > /proc/sys/vm/drop_caches
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

(Continued on next page)
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SPECspeed®2017_int_peak = 11.4

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

General Notes (Continued)

Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
UPI Link Enablement set to 1
UPI Power Management set to Enabled
Sub NUMA Clustering set to Disabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDCC Sparing set to Disabled
Patrol Scrub set to Disabled
Enhanced CPU performance set to Auto
Energy Efficient Turbo set to Enabled
Processor C6 Report set to Enabled
Processor C1E set to Enabled
Intel HyperThreading Technology set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d
running on localhost Tue Aug  3 08:32:27 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4314 CPU @ 2.40GHz
  2  "physical id"s (chips)
  32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 16
siblings : 16
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lscpu from util-linux 2.33.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 32
On-line CPU(s) list: 0-31

(Continued on next page)
### Platform Notes (Continued)

- Thread(s) per core: 1
- Core(s) per socket: 16
- Socket(s): 2
- NUMA node(s): 2
- Vendor ID: GenuineIntel
- CPU family: 6
- Model: 106
- Model name: Intel(R) Xeon(R) Silver 4314 CPU @ 2.40GHz
- Stepping: 6
- CPU MHz: 800.000
- CPU max MHz: 3400.0000
- CPU min MHz: 800.0000
- BogoMIPS: 4800.00
- Virtualization: VT-x
- L1d cache: 48K
- L1i cache: 32K
- L2 cache: 1280K
- L3 cache: 24576K
- NUMA node0 CPU(s): 0-15
- NUMA node1 CPU(s): 16-31
- Flags: fpu vme de pse tec msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nop1 xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pclid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invvpcl_single ssbd mba ibrs ibpb intel_pstate ibrs_ha ibrs_enhanced tpr_shadow vnumi flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 emms invpcid_single ssbd mba ibrs ibpb intel_pstate ibrs_ha ibrs_enhanced tpr_shadow vnumi flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 emms invpcid_single ssbd mba ibrs ibpb intel_pstate ibrs_ha ibrs_enhanced tpr_shadow vnumi flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 emms invpcid_single ssbd mba ibrs ibpb intel_pstate ibrs_ha ibrs_enhanced tpr_shadow vnumi flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 emms invpcid_single ssbd mba ibrs ibpb intel_pstate ibrs_ha ibrs_enhanced tpr_shadow vnumi flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 emms invpcid_single ssbd mba ibrs ibpb intel_pstate ibrs_ha ibrs_enhanced tpr_shadow vnumi flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 emms invpcid_single ssbd mba ibrs ibpb intel_pstate ibrs_ha ibrs_enhanced tpr_shadow vnumi flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 emms invpcid_single ssbd mba ibrs ibpb intel_pstate ibrs_ha ibrs_enhanced tpr_shadow vnumi flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 emms invpcid_single ssbd mba ibrs ibpb intel_pstate ibrs_ha ibrs_enhanced tpr_shadow vnumi flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 emms invpcid_single ssbd mba ibrs ibpb intel_pstate ibrs_ha ibrs_enhanced tpr_shadow vnumi flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 emms invpcid_single ssbd mba ibrs ibpb intel_pstate ibrs_ha ibrs_enhanced tpr_shadow vnumi flexpriority ept_vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 emms invpcid_single ssbd mba ibrs ibpb intel_pstate ibrs_ha ibrs_enhanced tpr_shadow vnumi flexpriority ept_vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 emms invpcid_single ssbd mba ibrs ibpb intel_pstate ibrs_ha ibrs_enhanced tpr_shadow vnumi flexpriority ept_vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 emms invpcid_single ssbd mba ibrs ibpb intel_pstate ibrs_ha ibrs_enhanced tpr_shadow vnumi flexpriority ept_vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 emms invpcid_single ssbd mba ibrs ibpb intel_pstate ibrs_ha ibrs_enhanced tpr_shadow vnumi flexpriority ept_vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 emms invpcid_single ssbd mba ibrs ibpb intel_pstate ibrs_ha ibrs_enhanced tpr_shadow vnumi flexpriority ept_vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 emms invpcid_single ssbd mba ibrs ibpb intel_pstate ibrs_ha ibrs_enhanced tpr_shadow vnumi flexpriority ept_vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 emms invpcid_single ssbd mba ibrs ibpb intel_pstate ibrs_ha ibrs_enhanced tpr_shadow vnumi flexpriority ept_vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 emms invpcid_single ssbd mba ibrs ibpb intel_pstate ibrs_ha ibrs_enhanced tpr_shadow vnumi flexpriority ept_vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 emms invpcid_single ssbd mba ibrs ibpb intel_pstate ibrs_ha ibrs_enhanced tpr_shadow vnumi flexpriority ept_vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 emms invpcid_single ssbd mba ibrs ibpb intel_pstate ibrs_ha ibrs_enhanced tpr_shadow vnumi flexpriority ept_vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 emms invpcid_36

From numactl --hardware

**WARNING:** A numactl 'node' might or might not correspond to a physical chip.

- available: 2 nodes (0-1)
- node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
- node 0 size: 515579 MB
- node 0 free: 509540 MB
- node 1 cpus: 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
- node 1 size: 515814 MB
- node 1 free: 505052 MB

(Continued on next page)
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SPECspeed®2017_int_base = 11.1
SPECspeed®2017_int_peak = 11.4

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Platform Notes (Continued)

node distances:
node 0 1
0: 10 20
1: 20 10

From /proc/meminfo
MemTotal: 1056147284 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15-SP2"
VERSION_ID="15.2"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
Linux localhost 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2018-3639 (Speculative Store Bypass): Mitigation: usercopy/swapgs barriers and __user pointer sanitization
CVE-2017-5753 (Spectre variant 1): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2017-5715 (Spectre variant 2): Not affected
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Aug 3 03:32

(Continued on next page)
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CPU2017 License: 9019
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Platform Notes (Continued)
---

SPEC is set to: /home/cpu2017
Filesystem    Type Size  Used Avail Use% Mounted on
/dev/sda2     btrfs 222G  46G  175G 21% /home

From /sys/devices/virtual/dmi/id
Vendor: Cisco Systems Inc
Product: UCSC-C220-M6S
Serial: WZP24430N7F

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
32x 0xCE00 M393A4K40DB3-CWE 32 GB 2 rank 3200, configured at 2666

BIOS:
BIOS Vendor: Cisco Systems, Inc.
BIOS Version: C220M6.4.2.1.c.1.0701210708
BIOS Date: 07/01/2021
BIOS Revision: 5.22

(End of data from sysinfo program)

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Compiler Version Notes
---

C       | 600.perlbench_s(peak)
--------------------------

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

--------------------------

C       | 600.perlbench_s(base) 602.gcc_s(base, peak) 605.mcf_s(base, peak)
| 625.x264_s(base, peak) 657.xz_s(base, peak)
--------------------------

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

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C       | 600.perlbench_s(peak)
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Compiler Version Notes (Continued)

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================
C       | 600.perlbench_s(base) 602.gcc_s(base, peak) 605.mcf_s(base, peak)
| 625.x264_s(base, peak) 657.xz_s(base, peak)
==============================================================================
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================
C++     | 620.omnetpp_s(base, peak) 623.xalancbmk_s(base, peak)
| 631.deepsjeng_s(base, peak) 641.leela_s(base, peak)
==============================================================================
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================
Fortran | 648.exchange2_s(base, peak)
==============================================================================
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================

Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort
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**Base Portability Flags**

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

**Base Optimization Flags**

C benchmarks:

C++ benchmarks:

Fortran benchmarks:
-m64 -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte -auto -mbranches-within-32B-boundaries

**Peak Compiler Invocation**

C benchmarks (except as noted below):
icx

600.perlbench_s: icc

C++ benchmarks:
icpx

(Continued on next page)
Cisco Systems  
Cisco UCS C220 M6 (Intel Xeon Silver 4314, 2.40GHz)  

SPECspeed®2017_int_base = 11.1  
SPECspeed®2017_int_peak = 11.4

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems  
Test Date: Aug-2021  
Hardware Availability: Apr-2021  
Software Availability: Dec-2020

Peak Compiler Invocation (Continued)

Fortran benchmarks: ifort

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:

600.perlbench_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)  
-xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4 -fno-strict-overflow  
-mbranches-within-32B-boundaries  
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

602.gcc_s: -m64 -std=c11 -Wl,-z,muldefs -fprofile-generate(pass 1)  
-fprofile-use=default.profdata(pass 2) -xCORE-AVX512 -flto  
-Ofast(pass 1) -O3 -ffast-math -qopt-mem-layout-trans=4  
-mbranches-within-32B-boundaries  
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

605.mcf_s: basepeak = yes

625.x264_s: -DSPEC_OPENMP -fiopenmp -std=c11 -m64 -Wl,-z,muldefs  
-xCORE-AVX512 -flto -O3 -ffast-math  
-qopt-mem-layout-trans=4 -fno-alias  
-mbranches-within-32B-boundaries  
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

657.xz_s: basepeak = yes

C++ benchmarks:

620.omnetpp_s: basepeak = yes

623.xalancbmk_s: basepeak = yes

631.deepsjeng_s: basepeak = yes

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Silver 4314, 2.40GHz)  

<table>
<thead>
<tr>
<th>SPECspeed®2017_int_base</th>
<th>SPECspeed®2017_int_peak</th>
</tr>
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<tbody>
<tr>
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</table>

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems  
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Software Availability: Dec-2020

**Peak Optimization Flags (Continued)**

641.leela_s: basepeak = yes

Fortran benchmarks:

648.exchange2_s: basepeak = yes

The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links:


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