Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 5318S, 2.10GHz)

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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

600.perlbench_s 48
602.gcc_s 48
605.mcf_s 48
620.omnetpp_s 48
623.xalancbmk_s 48
625.x264_s 48
631.deepsjeng_s 48
641.leela_s 48
648.exchange2_s 48
657.xz_s 48

**Hardware**

CPU Name: Intel Xeon Gold 5318S
Max MHz: 3400
Nominal: 2100
Enabled: 48 cores, 2 chips
Orderable: 1.2 Chips
Cache L1: 32 KB I + 48 KB D on chip per core
L2: 1.25 MB I+D on chip per core
L3: 36 MB I+D on chip per chip
Other: None
Memory: 1 TB (32 x 32 GB 2Rx4 PC4-3200V-R, running at 2933)
Storage: 1 x 300 GB 15K SAS HDD
Other: None

**Software**

OS: SUSE Linux Enterprise Server 15 SP2
Version: 5.3.18-22-default
Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux;
Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux;
C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux
Parallel: Yes
Firmware: Version 4.2.1c released Jul-2021
File System: btrfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS and OS set to prefer performance at the cost of additional power usage

---

SPEC CPU®2017 Integer Speed Result

**SPEC Speed®2017 int_base = 11.4**

**SPEC Speed®2017 int_peak = 11.6**
## SPEC CPU®2017 Integer Speed Result

**Cisco Systems**  
Cisco UCS C220 M6 (Intel Xeon Gold 5318S, 2.10GHz)  

**SPECspeed®2017_int_base = 11.4**  
**SPECspeed®2017_int_peak = 11.6**

### Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>48</td>
<td>256</td>
<td>6.92</td>
<td>255</td>
<td>6.97</td>
<td>255</td>
<td>6.96</td>
<td>48</td>
<td>224</td>
<td>7.93</td>
<td>223</td>
<td>7.95</td>
<td>223</td>
<td>7.96</td>
<td></td>
<td></td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>48</td>
<td>379</td>
<td>10.5</td>
<td>378</td>
<td>10.5</td>
<td>378</td>
<td>10.5</td>
<td>48</td>
<td>367</td>
<td>10.8</td>
<td>365</td>
<td>10.9</td>
<td>365</td>
<td>10.9</td>
<td></td>
<td></td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>48</td>
<td>248</td>
<td>19.0</td>
<td>248</td>
<td>19.1</td>
<td>249</td>
<td>19.0</td>
<td>48</td>
<td>248</td>
<td>19.0</td>
<td>248</td>
<td>19.1</td>
<td>249</td>
<td>19.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>48</td>
<td>154</td>
<td>10.6</td>
<td>152</td>
<td>10.8</td>
<td>159</td>
<td>10.3</td>
<td>48</td>
<td>154</td>
<td>10.6</td>
<td>152</td>
<td>10.8</td>
<td>159</td>
<td>10.3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>625.x264_s</td>
<td>48</td>
<td>107</td>
<td>16.5</td>
<td>108</td>
<td>16.4</td>
<td>107</td>
<td>16.5</td>
<td>48</td>
<td>103</td>
<td>17.1</td>
<td>103</td>
<td>17.2</td>
<td>103</td>
<td>17.2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>48</td>
<td>249</td>
<td>5.75</td>
<td>249</td>
<td>5.75</td>
<td>249</td>
<td>5.76</td>
<td>48</td>
<td>249</td>
<td>5.75</td>
<td>249</td>
<td>5.75</td>
<td>249</td>
<td>5.75</td>
<td></td>
<td></td>
</tr>
<tr>
<td>641.leela_s</td>
<td>48</td>
<td>359</td>
<td>4.75</td>
<td>362</td>
<td>4.71</td>
<td>359</td>
<td>4.75</td>
<td>48</td>
<td>359</td>
<td>4.75</td>
<td>362</td>
<td>4.71</td>
<td>359</td>
<td>4.75</td>
<td></td>
<td></td>
</tr>
<tr>
<td>648.exchange2_s</td>
<td>48</td>
<td>156</td>
<td>18.8</td>
<td>156</td>
<td>18.8</td>
<td>156</td>
<td>18.8</td>
<td>48</td>
<td>156</td>
<td>18.8</td>
<td>156</td>
<td>18.8</td>
<td>156</td>
<td>18.8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>657.xz_s</td>
<td>48</td>
<td>275</td>
<td>22.5</td>
<td>277</td>
<td>22.3</td>
<td>275</td>
<td>22.5</td>
<td>48</td>
<td>275</td>
<td>22.5</td>
<td>277</td>
<td>22.3</td>
<td>275</td>
<td>22.5</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**SPECspeed®2017_int_base = 11.4**  
**SPECspeed®2017_int_peak = 11.6**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:
- KMP_AFFINITY = "granularity=fine,scatter"
- LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
- MALLOC_CONF = "retain:true"
- OMP_STACKSIZE = "192M"

### General Notes

Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM memory using Redhat Enterprise Linux 8.0

Transparent Huge Pages enabled by default

Prior to runcpu invocation:
Filesystem page cache synced and cleared with:

```
sync; echo 3> /proc/sys/vm/drop_caches
```

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

(Continued on next page)
General Notes (Continued)


Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
UPI Link Enablement set to 1
UPI Power Management set to Enabled
Sub NUMA Clustering set to Disabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDDC Sparing set to Disabled
Patrol Scrub set to Disabled
Enhanced CPU performance set to Auto
Energy Efficient Turbo set to Enabled
Processor C6 Report set to Enabled
Processor C1E set to Enabled
Intel HyperThreading Technology set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16aca6c64
running on localhost Fri Aug 13 23:18:20 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 5318S CPU @ 2.10GHz
  2 "physical id"s (chips)
  48 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 24
siblings : 24
  physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
  physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23

From lscpu from util-linux 2.33.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 48
On-line CPU(s) list: 0-47

(Continued on next page)
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Test Date: Aug-2021
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Platform Notes (Continued)

Thread(s) per core: 1
Core(s) per socket: 24
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Gold 5318S CPU @ 2.10GHz
Stepping: 6
CPU MHz: 831.184
CPU max MHz: 3400.0000
CPU min MHz: 800.0000
BogoMIPS: 4200.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 36864K
NUMA node0 CPU(s): 0-23
NUMA node1 CPU(s): 24-47
Flags: fpu vme vmx pse mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pccid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat _13 invpcid_single ssbd mba ibrs ibpb ibrs_enhanced tpr_shadow vmi flexpriority ept vpid ept_ad fsbigpage tsc_adjust bmi1 hle avx2 smep bmi2 erms invvpid rtm cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha ni avx512bw avx512vl xsaveopt xsaves xsavec xsaveopt xsaves cqm_llc cqm_occuppy_llc cqm_mbb_total cqm_mbb_local wbnoivd dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req avx512vmbi umip pku ospke avx512_vbmi2 gfnl vaes vpclmulqdq avx512_vnni avx512_bitalg tme avx512_vpopcntdq la57 rdpid md_clear pconfig flush_l1d arch_capabilities

From numacl --hardware

WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
node 0 size: 515649 MB
node 0 free: 515086 MB
node 1 cpus: 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47
node 1 size: 515649 MB
node 1 free: 515086 MB

(Continued on next page)
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Platform Notes (Continued)

node distances:
node  0  1
   0:  10  20
   1:  20  10

From /proc/meminfo
MemTotal:       1056498052 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES" 
    VERSION="15-SP2"
    VERSION_ID="15.2"
    PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15:sp2"

  uname -a:
  Linux localhost 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
  x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs barriers and __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Aug 13 23:11

(Continued on next page)
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Platform Notes (Continued)

SPEC is set to: /home/cpu2017
Filesystem    Type   Size  Used  Avail  Use% Mounted on
/dev/sda2     btrfs 222G  31G  190G  14% /home

From /sys/devices/virtual/dmi/id
Vendor:       Cisco Systems Inc
Product:      UCSC-C220-M6S
Serial:       WZP24430ADF

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
32x 0xCE00 M393A4K40DB3-CWE 32 GB 2 rank 3200, configured at 2933

BIOS:
BIOS Vendor:   Cisco Systems, Inc.
BIOS Version:  C220M6.4.2.1c.1.0701210708
BIOS Date:     07/01/2021
BIOS Revision: 5.22

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C       | 600.perlbench_s(peak)
==============================================================================
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================

==============================================================================
C       | 600.perlbench_s(base) 602.gcc_s(base, peak) 605.mcf_s(base, peak)
       | 625.x264_s(base, peak) 657.xz_s(base, peak)
==============================================================================
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================

C       | 600.perlbench_s(peak)
(Continued on next page)
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Compiler Version Notes (Continued)

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
==============================================================================
C       | 600.perlbench_s(base) 602.gcc_s(base, peak) 605.mcf_s(base, peak) 625.x264_s(base, peak) 657.xz_s(base, peak)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
==============================================================================
C++     | 620.omnetpp_s(base, peak) 623.xalancbmk_s(base, peak) 631.deepsjeng_s(base, peak) 641.leela_s(base, peak)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
==============================================================================
Fortran | 648.exchange2_s(base, peak)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort
## Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 5318S, 2.10GHz)

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<tr>
<th>SPECspeed®2017_int_base</th>
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## Base Portability Flags

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<tr>
<th>Benchmark</th>
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</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s:</td>
<td>-DSPEC_LP64 -DSPEC_LINUX_X64</td>
</tr>
<tr>
<td>602.gcc_s:</td>
<td>-DSPEC_LP64</td>
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</tr>
<tr>
<td>657.xz_s:</td>
<td>-DSPEC_LP64</td>
</tr>
</tbody>
</table>

## Base Optimization Flags

### C benchmarks:
-DSPEC_OPENMP -std=c11 -m64 -fiopenmp -Wl,-z,muldefs -xCORE-AVX512
-03 -ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

### C++ benchmarks:
-DSPEC_OPENMP -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin/
-1qkmalloc

### Fortran benchmarks:
-m64 -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto
-mbranches-within-32B-boundaries

## Peak Compiler Invocation

### C benchmarks (except as noted below):
icx

600.perlbench_s: icc

### C++ benchmarks:
icpx

(Continued on next page)
Peak Compiler Invocation (Continued)

Fortran benchmarks:
ifort

Peak Portability Flags
Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:

600.perlbench_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)
-xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-strict-overflow
-mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

602.gcc_s: -m64  -std=c11 -Wl,-z,muldefs -fprofile-generate(pass 1)
-fprofile-use=default.profdata(pass 2) -xCORE-AVX512 -flto
-Ofast(pass 1) -O3 -ffast-math -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

605.mcf_s: basepeak = yes

625.x264_s: -DSPEC_OPENMP -fopenmp -std=c11 -m64 -Wl,-z,muldefs
-xCORE-AVX512 -flto -O3 -ffast-math
-qopt-mem-layout-trans=4 -fno-alias
-mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

657.xz_s: basepeak = yes

C++ benchmarks:

620.omnetpp_s: basepeak = yes

623.xalancbmk_s: basepeak = yes

631.deepsjeng_s: basepeak = yes

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Peak Optimization Flags (Continued)

641.leela_s: basepeak = yes

Fortran benchmarks:
648.exchange2_s: basepeak = yes

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.8 on 2021-08-13 23:18:20-0400.
Report generated on 2021-09-01 14:25:48 by CPU2017 PDF formatter v6442.
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