### Cisco Systems

Cisco UCS C240 M6 (Intel Xeon Silver 4310, 2.10GHz)

<table>
<thead>
<tr>
<th>Software</th>
<th>SPECspeak®2017_int_base = 10.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Date:</td>
<td>Aug-2021</td>
</tr>
<tr>
<td>Hardware Availability:</td>
<td>Jan-2021</td>
</tr>
</tbody>
</table>

#### Hardware

- **CPU Name:** Intel Xeon Silver 4310
- **Max MHz:** 3300
- **Nominal:** 2100
- **Enabled:** 24 cores, 2 chips
- **Orderable:** 1,2 Chips
- **Cache L1:** 32 KB I + 48 KB D on chip per core
- **L2:** 1.25 MB I+D on chip per core
- **L3:** 18 MB I+D on chip per chip
- **Other:** None
- **Memory:** 2 TB (32 x 64 GB 2Rx4 PC4-3200V-R, running at 2666)
- **Storage:** 1 x 240 GB SATA SSD
- **Other:** None

#### Software

- **OS:** SUSE Linux Enterprise Server 15 SP2 5.3.18-22-default
- **Compiler:** C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux; Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux
- **Parallel:** Yes
- **Firmware:** Version 4.2.1c released Jul-2021
- **File System:** btrfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** Not Applicable
- **Other:** jemalloc memory allocator V5.0.1
- **Power Management:** BIOS and OS set to prefer performance at the cost of additional power usage

#### SPEC CPU®2017 Integer Speed Result

<table>
<thead>
<tr>
<th>SPECspeak®2017_int_peak = Not Run</th>
</tr>
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<tbody>
<tr>
<td>SPECspeak®2017_int_base = 10.5</td>
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<tr>
<td>Threads</td>
</tr>
<tr>
<td>600.perbench_s 24 6.68</td>
</tr>
<tr>
<td>602.gcc_s 24 9.82</td>
</tr>
<tr>
<td>605.mcf_s 24 18.3</td>
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<tr>
<td>620.omnetpp_s 24 7.89</td>
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<tr>
<td>623.xalancbmk_s 24 12.6</td>
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<td>625.x264_s 24 15.6</td>
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<tr>
<td>631.deepsjeng_s 24 5.59</td>
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<tr>
<td>641.leela_s 24 4.61</td>
</tr>
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<td>648.exchange2_s 24 18.2</td>
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<tr>
<td>657.xz_s 24 19.4</td>
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**Test Sponsor:** Cisco Systems
**Hardware** Availability: Jan-2021
**Software** Availability: Jan-2021
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**Cisco Systems**  
Cisco UCS C240 M6 (Intel Xeon Silver 4310, 2.10GHz)  

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**CPU2017 License:** 9019  
**Test Date:** Aug-2021  
**Test Sponsor:** Cisco Systems  
**Hardware Availability:** Jun-2021  
**Tested by:** Cisco Systems  
**Software Availability:** Mar-2021

### Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Base</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Peak</th>
<th>Seconds</th>
<th>Ratio</th>
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<tr>
<td>perlbench_s</td>
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<td>gcc_s</td>
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<td>406</td>
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<td>404</td>
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<td>18.3</td>
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<td>xalancbmk_s</td>
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<td>12.6</td>
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<td>12.6</td>
<td>113</td>
<td>12.6</td>
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<td></td>
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<tr>
<td>x264_s</td>
<td>24</td>
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<td>15.6</td>
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<td>15.6</td>
<td>113</td>
<td>15.6</td>
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<tr>
<td>deepsjeng_s</td>
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<tr>
<td>exchange2_s</td>
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<td>18.2</td>
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<tr>
<td>xz_s</td>
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<td>319</td>
<td>19.4</td>
<td>319</td>
<td>19.4</td>
<td>319</td>
<td>19.4</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:
- KMP_AFFINITY = "granularity=fine,scatter"
- LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
- MALLOC_CONF = "retain:true"
- OMP_STACKSIZE = "192M"

### General Notes

Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM  
memory using openSUSE Leap 15.2  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation  
Filesystem page cache synced and cleared with:  
sync; echo 3>/proc/sys/vm/drop_caches  
runcpu command invoked through numactl i.e.:

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Silver 4310, 2.10GHz)

SPECspeed\textsuperscript{\textregistered}2017\_int\_base = 10.5
SPECspeed\textsuperscript{\textregistered}2017\_int\_peak = Not Run

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
<th>Test Date:</th>
<th>Aug-2021</th>
</tr>
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<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
<td>Hardware Availability:</td>
<td>Jun-2021</td>
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<td>Cisco Systems</td>
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</table>

General Notes (Continued)

numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel Hyper-Threading Technology set to Disabled
DCU Streamer Prefetch set to Disabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDDC Sparing set to Disabled
Patrol Scrub set to Disabled
Processor C6 Report set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acaf64d
running on localhost Mon Aug 16 05:04:20 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Silver 4310 CPU @ 2.10GHz
  2 "physical id"s (chips)
  24 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 12
siblings : 12
  physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11
  physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11

From lscpu from util-linux 2.33.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual

(Continued on next page)
Cisco Systems
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECspeed®2017_int_base = 10.5
SPECspeed®2017_int_peak = Not Run

CPU(s): 24
On-line CPU(s) list: 0-23
Thread(s) per core: 1
Core(s) per socket: 12
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Silver 4310 CPU @ 2.10GHz
Stepping: 6
CPU MHz: 2692.125
CPU max MHz: 3300.0000
CPU min MHz: 800.0000
BogoMIPS: 4200.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 18432K
NUMA node0 CPU(s): 0-11
NUMA node1 CPU(s): 12-23
Flags: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 invpcid_single ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vmpnop flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 耸m invpcid rtm cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha ni avx512bw avx512vl xsavesopt xsaveopt xsavevc xsavec cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local wbnoinvd dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req avx512vmbi umip pku ospke avx512_vbmi12 gfni vaes vpclmulqdq avx512_vnni avx512_bitalg tme avx512_vpopcntdq 5a57 rdpid md_clear pconfig flush_l1d arch_capabilities

/cache data
   cache size: 18432 KB

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
   available: 2 nodes (0-1)
   node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11
   node 0 size: 1031781 MB
   node 0 free: 1030948 MB
   node 1 cpus: 12 13 14 15 16 17 18 19 20 21 22 23

(Continued on next page)
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</table>

### Platform Notes (Continued)

node 1 size: 1032151 MB  
node 1 free: 1027977 MB  
node distances:  
node 0 1  
0: 10 20  
1: 20 10

From `/proc/meminfo`  
MemTotal: 2113467328 kB  
HugePages_Total: 0  
Hugepagesize: 2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From `/etc/*release` /`/etc/*version`  
`NAME="SLES"`  
`VERSION="15-SP2"`  
`VERSION_ID="15.2"`  
`PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"`  
`ID="sles"`  
`ID_LIKE="suse"`  
`ANSI_COLOR="0;32"`  
`CPE_NAME="cpe:/o:suse:sles:15:sp2"`

`uname -a:`  
Linux localhost 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64  
x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

<table>
<thead>
<tr>
<th>CVE-2018-12207 (iTLB Multihit):</th>
<th>Not affected</th>
</tr>
</thead>
<tbody>
<tr>
<td>CVE-2018-3620 (L1 Terminal Fault):</td>
<td>Not affected</td>
</tr>
<tr>
<td>Microarchitectural Data Sampling:</td>
<td>Not affected</td>
</tr>
<tr>
<td>CVE-2017-5754 (Meltdown):</td>
<td>Mitigation: Speculative Store Bypass disabled via prctl and seccomp</td>
</tr>
<tr>
<td>CVE-2018-3639 (Speculative Store Bypass):</td>
<td>Mitigation: Speculative Store Bypass disabled via prctl and seccomp</td>
</tr>
<tr>
<td>CVE-2017-5753 (Spectre variant 1):</td>
<td>Mitigation: usercopy/swapgs barriers and __user pointer sanitization</td>
</tr>
<tr>
<td>CVE-2017-5715 (Spectre variant 2):</td>
<td>Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling</td>
</tr>
<tr>
<td>CVE-2020-0543 (Special Register Buffer Data Sampling):</td>
<td>Not affected</td>
</tr>
<tr>
<td>CVE-2019-11135 (TSX Asynchronous Abort):</td>
<td>Not affected</td>
</tr>
</tbody>
</table>

(Continued on next page)
## Platform Notes (Continued)

run-level 3 Aug 16 02:50

SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sdb2 btrfs 222G 17G 204G 8% /home

From /sys/devices/virtual/dmi/id

Vendor: Cisco Systems Inc
Product: UCSC-C240-M6S
Serial: WZP24460JDQ

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200, configured at 2666

BIOS:
- BIOS Vendor: Cisco Systems, Inc.
- BIOS Version: C240M6.4.2.1c.10.0723211453
- BIOS Date: 07/23/2021
- BIOS Revision: 5.22

(End of data from sysinfo program)

## Compiler Version Notes

```
-------------------------------------------------------------------------------
C       | 600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base) 625.x264_s(base) 657.xz_s(base)
-------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
-------------------------------------------------------------------------------

C++      | 620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base) 641.leela_s(base)
-------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
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```

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Copyright 2017-2021 Standard Performance Evaluation Corporation

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Compiler Version Notes (Continued)
==============================================================================
Fortran | 648.exchange2_s(base)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Base Compiler Invocation
C benchmarks:
icx
C++ benchmarks:
icpx
Fortran benchmarks:
ifort

Base Portability Flags
600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags
C benchmarks:
-DSPEC_OPENMP -std=c11 -m64 -fiopenmp -Wl,-z,muldefs -xCORE-AVX512
-O3 -ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

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### Base Optimization Flags (Continued)

**C++ benchmarks:**
-DSPEC_OPENMP -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math  
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4  
-mbranches-within-32B-boundaries  
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin/  
-1qkmalloc

**Fortran benchmarks:**
-m64 -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-mem-layout-trans=4  
-nostandard-realloc-lhs -align array32byte -auto  
-mbranches-within-32B-boundaries

The flags files that were used to format this result can be browsed at:

You can also download the XML flags sources by saving the following links:

---

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.8 on 2021-08-16 05:04:19-0400.  
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