Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Platinum 8368Q, 2.60GHz)  

SPECrate®2017_int_base = 507
SPECrate®2017_int_peak = 527

Copies

0  50.0  100  150  200  250  300  350  400  450  500  550  600  650  700  750  800  850  900  950  1000  1050  1100  1150

500.perlbench_r  152
502.gcc_r  152
505.mcf_r  152
520.omnetpp_r  152
523.xalancbmk_r  152
525.x264_r  152
531.deepsjeng_r  152
541.leela_r  152
548.exchange2_r  152
557.xz_r  152

SPECrate®2017_int_base (507)
SPECrate®2017_int_peak (527)

Hardware
CPU Name: Intel Xeon Platinum 8368Q
Max MHz: 3700
Nominal: 2600
Enabled: 76 cores, 2 chips, 2 threads/core
Orderable: 1.2 Chips
Cache L1: 32 KB I + 48 KB D on chip per core
L2: 1.25 MB I+D on chip per core
L3: 57 MB I+D on chip per chip
Other: None
Memory: 2 TB (32 x 64 GB 2Rx4 PC4-3200V-R)
Storage: 1 x 480 GB SATA SSD
Other: None

Software
OS: SUSE Linux Enterprise Server 15 SP2
5.3.18-22-default
Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++
Compiler Build 20201113 for Linux;
Fortran: Version 2021.1 of Intel Fortran Compiler
Classic Build 20201112 for Linux;
C/C++: Version 2021.1 of Intel C/C++ Compiler
Classic Build 20201112 for Linux
Parallel: No
Firmware: Version 4.2.1c released Jul-2021
File System: btrfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 32/64-bit
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS and OS set to prefer performance at the cost of additional power usage
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Platinum 8368Q, 2.60GHz)

SPECrate®2017_int_base = 507
SPECrate®2017_int_peak = 527

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Base Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Peak Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>152</td>
<td>687</td>
<td>352</td>
<td>685</td>
<td>353</td>
<td>685</td>
<td>353</td>
<td>152</td>
<td>580</td>
<td>417</td>
<td>590</td>
<td>410</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>152</td>
<td>554</td>
<td>388</td>
<td>555</td>
<td>388</td>
<td>557</td>
<td>387</td>
<td>152</td>
<td>454</td>
<td>474</td>
<td>452</td>
<td>476</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>152</td>
<td>294</td>
<td>836</td>
<td>296</td>
<td>831</td>
<td>294</td>
<td>834</td>
<td>152</td>
<td>294</td>
<td>836</td>
<td>296</td>
<td>831</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>152</td>
<td>692</td>
<td>288</td>
<td>693</td>
<td>288</td>
<td>694</td>
<td>288</td>
<td>152</td>
<td>692</td>
<td>288</td>
<td>693</td>
<td>288</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>152</td>
<td>254</td>
<td>633</td>
<td>251</td>
<td>639</td>
<td>250</td>
<td>643</td>
<td>152</td>
<td>254</td>
<td>633</td>
<td>251</td>
<td>639</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>152</td>
<td>253</td>
<td>1050</td>
<td>251</td>
<td>1060</td>
<td>255</td>
<td>1050</td>
<td>152</td>
<td>242</td>
<td>1100</td>
<td>241</td>
<td>1110</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>152</td>
<td>437</td>
<td>399</td>
<td>433</td>
<td>402</td>
<td>437</td>
<td>399</td>
<td>152</td>
<td>437</td>
<td>399</td>
<td>433</td>
<td>402</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>152</td>
<td>618</td>
<td>407</td>
<td>607</td>
<td>415</td>
<td>615</td>
<td>409</td>
<td>152</td>
<td>618</td>
<td>407</td>
<td>607</td>
<td>415</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>152</td>
<td>373</td>
<td>1070</td>
<td>367</td>
<td>1090</td>
<td>371</td>
<td>1070</td>
<td>152</td>
<td>373</td>
<td>1070</td>
<td>367</td>
<td>1090</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>152</td>
<td>569</td>
<td>288</td>
<td>568</td>
<td>289</td>
<td>565</td>
<td>291</td>
<td>152</td>
<td>572</td>
<td>287</td>
<td>568</td>
<td>289</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"
MALLOCONF = "retain:true"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
  sync; echo 3 > /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
**SPEC CPU®2017 Integer Rate Result**

**Cisco Systems**  
Cisco UCS B200 M6 (Intel Xeon Platinum 8368Q, 2.60GHz)  

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base = 507</th>
<th>SPECrate®2017_int_peak = 527</th>
</tr>
</thead>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**General Notes (Continued)**

```bash
numactl --interleave=all runcpu <etc>
```

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.


**Platform Notes**

**BIOS Settings:**
- Adjacent Cache Line Prefetcher set to Disabled
- DCU Streamer Prefetch set to Disabled
- UPI Link Enablement set to 1
- UPI Power Management set to Enabled
- Sub NUMA Clustering set to Enabled
- LLC Dead Line set to Disabled
- Memory Refresh Rate set to 1x Refresh
- ADDDC Sparing set to Disabled
- Patrol Scrub set to Disabled
- Enhanced CPU performance set to Disabled
- Energy Efficient Turbo set to Enabled
- Processor C6 Report set to Enabled
- Processor C1E set to Enabled

**Sysinfo program /home/cpu2017/bin/sysinfo**  
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d  
running on install Wed Aug 4 13:09:02 2021

SUT (System Under Test) info as seen by some common utilities.  
For more information on this section, see  
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo  
```
model name : Intel(R) Xeon(R) Platinum 8368Q CPU @ 2.60GHz
  2 "physical id"s (chips)
  152 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 38
siblings : 76
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37
```

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Platinum 8368Q, 2.60GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECrate®2017_int_base = 507
SPECrate®2017_int_peak = 527

Platform Notes (Continued)

physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37

From lscpu from util-linux 2.33.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 152
On-line CPU(s) list: 0-151
Thread(s) per core: 2
Core(s) per socket: 38
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Platinum 8368Q CPU @ 2.60GHz
Stepping: 6
CPU MHz: 1059.507
CPU max MHz: 3700.0000
CPU min MHz: 800.0000
BogoMIPS: 5200.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 58368K
NUMA node0 CPU(s): 0-37,76-113
NUMA node1 CPU(s): 38-75,114-151
Flags: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pbebs bs rep_good nopl xtopology nonstop-tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pclid dsuid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 invpcid single ssbd mba ibrs ibrs_enhanced tpr_shadow vnmi flexpriority ept vpid ept_ad fs speculation tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt intel_pt avx512cd sha_ni avx512bw avx512vl xsaveopt xsaves xsavec xgetbv1 xsave vcmp32 hle avx2 smep bmi2 erms invpcid rtm cqm rdt_a_avx512f_avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt_avx512cd_sha_ni_avx512bw_avx512vl_xsaveopt_xsavec_xgetbv1_xsave vcmp32

/proc/cpuinfo cache data
cache size : 58368 KB

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Platinum 8368Q, 2.60GHz)

SPEC CPU®2017 Integer Rate Result
Copyright 2017-2021 Standard Performance Evaluation Corporation

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>SPECrate®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>507</td>
<td>527</td>
</tr>
</tbody>
</table>

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

<table>
<thead>
<tr>
<th>Test Date</th>
<th>Hardware Availability</th>
<th>Software Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td>Aug-2021</td>
<td>Apr-2021</td>
<td>Dec-2020</td>
</tr>
</tbody>
</table>

Platform Notes (Continued)

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
  available: 2 nodes (0-1)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27
  28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94
  95 96 97 98 99 100 101 102 103 104 105 106 107 108 109 110 111 112 113
  node 0 size: 1031576 MB
  node 0 free: 1030837 MB
  node 1 cpus: 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62
  63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94
  95 96 97 98 99 100 101 102 103 104 105 106 107 108 109 110 111 112 113
  node 1 size: 1032170 MB
  node 1 free: 1031421 MB
  node distances:
  node 0 1
  0: 10 20
  1: 20 10

From /proc/meminfo
  MemTotal:       2113276908 kB
  HugePages_Total:       0
  Hugepagesize:       2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
  NAME="SLES"
  VERSION="15-SP2"
  VERSION_ID="15.2"
  PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
  ID="sles"
  ID_LIKE="suse"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
  Linux install 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
  x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected

(Continued on next page)
Cisco Systems

Cisco UCS B200 M6 (Intel Xeon Platinum 8368Q, 2.60GHz)

Copyright 2017-2021 Standard Performance Evaluation Corporation

SPEC CPU®2017 Integer Rate Result

Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Platinum 8368Q, 2.60GHz)

SPECrate®2017_int_base = 507
SPECrate®2017_int_peak = 527

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Platform Notes (Continued)

Microarchitectural Data Sampling:
CVE-2017-5754 (Meltdown):
CVE-2018-3639 (Speculative Store Bypass):

CVE-2017-5753 (Spectre variant 1):
CVE-2017-5715 (Spectre variant 2):
CVE-2020-0543 (Special Register Buffer Data Sampling):
CVE-2019-11135 (TSX Asynchronous Abort):

run-level 3 Aug 4 13:00
SPECl is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda2 btrfs 443G 41G 401G 10% /home

From /sys/devices/virtual/dmi/id
Vendor: Cisco Systems Inc
Product: UCSB-B200-M6
Serial: FCH24097570

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200

BIOS:
BIOS Vendor: Cisco Systems, Inc.
BIOS Version: B200M6.4.2.1c.10.0723211453
BIOS Date: 07/23/2021
BIOS Revision: 5.22

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
| C       | 500.perlbench_r(peak) 557.xz_r(peak) |
--------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
64, Version 2021.1 Build 20201112_000000

(Continued on next page)
**Cisco Systems**

Cisco UCS B200 M6 (Intel Xeon Platinum 8368Q, 2.60GHz)

<table>
<thead>
<tr>
<th>CPU2017 License: 9019</th>
<th>SPECrate®2017_int_base = 507</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor: Cisco Systems</td>
<td>SPECrate®2017_int_peak = 527</td>
</tr>
<tr>
<td>Tested by: Cisco Systems</td>
<td></td>
</tr>
</tbody>
</table>

**Compiler Version Notes (Continued)**

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

<table>
<thead>
<tr>
<th>C</th>
<th>502.gcc_r(peak)</th>
</tr>
</thead>
</table>

Intel(R) oneAPI DPC+/C++ Compiler for applications running on IA-32, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

<table>
<thead>
<tr>
<th>C</th>
<th>500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)</th>
</tr>
</thead>
</table>

Intel(R) oneAPI DPC+/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

<table>
<thead>
<tr>
<th>C</th>
<th>500.perlbench_r(peak) 557.xz_r(peak)</th>
</tr>
</thead>
</table>

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

<table>
<thead>
<tr>
<th>C</th>
<th>502.gcc_r(peak)</th>
</tr>
</thead>
</table>

Intel(R) oneAPI DPC+/C++ Compiler for applications running on IA-32, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

<table>
<thead>
<tr>
<th>C</th>
<th>500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)</th>
</tr>
</thead>
</table>

Intel(R) oneAPI DPC+/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

<table>
<thead>
<tr>
<th>C</th>
<th>500.perlbench_r(peak) 557.xz_r(peak)</th>
</tr>
</thead>
</table>

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Platinum 8368Q, 2.60GHz)

SPECRate®2017_int_base = 507
SPECRate®2017_int_peak = 527

Cisco Systems

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Compiler Version Notes (Continued)

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

--------------------------------------------------------
C       | 502.gcc_r(peak)
--------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

--------------------------------------------------------
C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
525.x264_r(base, peak) 557.xz_r(base)
--------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

--------------------------------------------------------
C++      | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base, peak)
531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
--------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

--------------------------------------------------------
Fortran | 548.exchange2_r(base, peak)
--------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icx

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Platinum 8368Q, 2.60GHz)

SPECraten\textsuperscript{®}2017\_int\_base = 507
SPECraten\textsuperscript{®}2017\_int\_peak = 527

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Base Compiler Invocation (Continued)

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Base Portability Flags

500.perlbench\_r: -DSPEC\_LP64 -DSPEC\_LINUX\_X64
502.gcc\_r: -DSPEC\_LP64
505.mcf\_r: -DSPEC\_LP64
520.omnetpp\_r: -DSPEC\_LP64
523.xalancbmk\_r: -DSPEC\_LP64 -DSPEC\_LINUX
525.x264\_r: -DSPEC\_LP64
531.deepsjeng\_r: -DSPEC\_LP64
541.leela\_r: -DSPEC\_LP64
548.exchange2\_r: -DSPEC\_LP64
557.xz\_r: -DSPEC\_LP64

Base Optimization Flags

C benchmarks:
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

C++ benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

Fortran benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-auto -mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Platinum 8368Q, 2.60GHz)  

**SPECrate®2017_int_base = 507**  
**SPECrate®2017_int_peak = 527**

<table>
<thead>
<tr>
<th>CPU2017 License</th>
<th>Test Date</th>
<th>Test Sponsor</th>
<th>Hardware Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td>9019</td>
<td>Aug-2021</td>
<td>Cisco Systems</td>
<td>Apr-2021</td>
</tr>
<tr>
<td>Test by:</td>
<td>Software Availability:</td>
<td></td>
<td>Dec-2020</td>
</tr>
<tr>
<td>Cisco Systems</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Peak Compiler Invocation

C benchmarks (except as noted below):
- icx
- 500.perlbench_r:icc
- 557.xz_r:icc

C++ benchmarks:
- icpx

Fortran benchmarks:
- ifort

### Peak Portability Flags

- 500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
- 502.gcc_r: -D_FILE_OFFSET_BITS=64
- 505.mcf_r: -DSPEC_LP64
- 520.omnetpp_r: -DSPEC_LP64
- 523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
- 525.x264_r: -DSPEC_LP64
- 531.deepsjeng_r: -DSPEC_LP64
- 541.leela_r: -DSPEC_LP64
- 548.exchange2_r: -DSPEC_LP64
- 557.xz_r: -DSPEC_LP64

### Peak Optimization Flags

C benchmarks:
- 500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4 -fno-strict-overflow -mbranches-within-32B-boundaries
- L=/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin -lqkmalloc

- 502.gcc_r: -m32
- L=/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/ia32_lin
- -std=gnu89 -Wl,-z,muldefs -fprofile-generate(pass 1)
- -fprofile-use=default.profdata(pass 2) -xCORE-AVX512 -flto
- -Ofast(pass 1) -O3 -ffast-math -qopt-mem-layout-trans=4

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Platinum 8368Q, 2.60GHz)

SPECrate®2017_int_base = 507
SPECrate®2017_int_peak = 527

CPU2017 License: 9019
Test Date: Aug-2021
Test Sponsor: Cisco Systems
Hardware Availability: Apr-2021
Tested by: Cisco Systems
Software Availability: Dec-2020

Peak Optimization Flags (Continued)

502.gcc_r (continued):
-mbranches-within-32B-boundaries
-L/usr/local/jemalloc32-5.0.1/lib -ljemalloc

505.mcf_r: basepeak = yes

525.x264_r: -w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -flto
-O3 -ffast-math -qopt-mem-layout-trans=4 -fno-alias
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

557.xz_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

C++ benchmarks:

520.omnetpp_r: basepeak = yes
523.xalancbmk_r: basepeak = yes
531.deepsjeng_r: basepeak = yes
541.leela_r: basepeak = yes

Fortran benchmarks:

548.exchange2_r: basepeak = yes

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.8 on 2021-08-04 13:09:01-0400.
Report generated on 2021-09-01 14:23:54 by CPU2017 PDF formatter v6442.
Originally published on 2021-08-31.