SPEC CPU®2017 Floating Point Speed Result

Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Platinum 8368Q, 2.60GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jul-2021
Hardware Availability: Apr-2021
Software Availability: Dec-2020

Threads

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Value</th>
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<tbody>
<tr>
<td>603.bwaves_s</td>
<td>293</td>
</tr>
<tr>
<td>607.cactuBSSN_s</td>
<td>293</td>
</tr>
<tr>
<td>619.lbm_s</td>
<td>141</td>
</tr>
<tr>
<td>621.wrf_s</td>
<td>215</td>
</tr>
<tr>
<td>627.cam4_s</td>
<td>177</td>
</tr>
<tr>
<td>628.pop2_s</td>
<td>95.6</td>
</tr>
<tr>
<td>638.imagick_s</td>
<td>250</td>
</tr>
<tr>
<td>644.nab_s</td>
<td>506</td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
<td>255</td>
</tr>
<tr>
<td>654.roms_s</td>
<td>255</td>
</tr>
</tbody>
</table>

--- SPECspeed®2017_fp_base (228) ---

Hardware

CPU Name: Intel Xeon Platinum 8368Q
Max MHz: 3700
Nominal: 2600
Enabled: 76 cores, 2 chips
Orderable: 1.2 Chips
Cache L1: 32 KB I + 48 KB D on chip per core
Cache L2: 1.25 MB I+D on chip per core
Cache L3: 57 MB I+D on chip per chip
Other: None
Memory: 2 TB (32 x 64 GB 2Rx4 PC4-3200AA-R)
Storage: 1 x 240 GB SATA SSD
Other: None

Software

OS: SUSE Linux Enterprise Server 15 SP2
5.3.18-22-default
Compiler: Fortran: Version 2021.1 of Intel Fortran Compiler
Classic Build 20201112 for Linux;
C/C++: Version 2021.1 of Intel C/C++ Compiler
Classic Build 20201112 for Linux
Parallel: Yes
Firmware: Version 4.2.1c released Jul-2021
File System: btrfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS and OS set to prefer performance at the cost of additional power usage
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Platinum 8368Q, 2.60GHz)

SPECspeed®2017_fp_base = 228
SPECspeed®2017_fp_peak = Not Run

Results Table

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<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
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<tr>
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<td></td>
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<td>607.cactuBSSN_s</td>
<td>76</td>
<td>56.6</td>
<td>294</td>
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<tr>
<td>619.lbm_s</td>
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<td>627.cam4_s</td>
<td>76</td>
<td>50.0</td>
<td>177</td>
<td>51.3</td>
<td>173</td>
<td>49.6</td>
<td>179</td>
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<td>628.pop2_s</td>
<td>76</td>
<td>124</td>
<td>96.0</td>
<td>127</td>
<td>93.2</td>
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<tr>
<td>649.fotonik3d_s</td>
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<td>654.roms_s</td>
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<td>254</td>
<td>61.6</td>
<td>255</td>
<td><strong>61.8</strong></td>
<td><strong>255</strong></td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
- KMP_AFFINITY = "granularity=fine,compact"
- LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
- MALLOC_CONF = "retain:true"
- OMP_STACKSIZE = "192M"

General Notes
Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3 > /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:

(Continued on next page)
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Cisco UCS C240 M6 (Intel Xeon Platinum 8368Q, 2.60GHz)

SPEC CPU®2017 Floating Point Speed Result
Copyright 2017-2021 Standard Performance Evaluation Corporation

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<th>Jul-2021</th>
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<td>Hardware Availability:</td>
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<td>Tested by:</td>
<td>Cisco Systems</td>
<td>Software Availability:</td>
<td>Dec-2020</td>
</tr>
</tbody>
</table>

**General Notes (Continued)**

```
numactl --interleave=all runcpu <etc>
```

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.


---

**Platform Notes**

**BIOS Settings:**
- Intel Hyper-Threading Technology set to Disabled
- Adjacent Cache Line Prefetcher set to Disabled
- DCU Streamer Prefetch set to Disabled
- UPI Link Enablement set to 1
- UPI Power Management set to Enabled
- LLC Dead Line set to Disabled
- Memory Refresh Rate set to 1x Refresh
- ADDDC Sparing set to Disabled
- Patrol Scrub set to Disabled
- Enhanced CPU performance set to Auto
- Energy Efficient Turbo set to Enabled
- Processor C6 Report set to Enabled
- Processor C1E set to Enabled

`Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d
running on install Wed Jul 28 12:37:48 2021`

**SUT (System Under Test) info as seen by some common utilities.**
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

**From /proc/cpuinfo**

```
model name : Intel(R) Xeon(R) Platinum 8368Q CPU @ 2.60GHz
  2 "physical id"s (chips)
  76 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 38
siblings : 38
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37
```

(Continued on next page)
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SPECspeed®2017_fp_base = 228

SPECspeed®2017_fp_peak = Not Run

CPU2017 License: 9019
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Platform Notes (Continued)

physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37

From lscpu from util-linux 2.33.1:

Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 76
On-line CPU(s) list: 0-75
Thread(s) per core: 1
Core(s) per socket: 38
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Platinum 8368Q CPU @ 2.60GHz
Stepping: 6
CPU MHz: 3578.129
CPU max MHz: 3700.0000
CPU min MHz: 800.0000
BogoMIPS: 5200.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 58368K
NUMA node0 CPU(s): 0-37
NUMA node1 CPU(s): 38-75
Flags: fpu vmx vme de pse tsc msr pae mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 invpcid_single ssbd mba ibrs ibpb ibrs_enhanced tpr_shadow vnmi flexpriority ept vpid ept_ad fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha_ni avx512bw avx512vl xsaveopt xsaves xSAVEc xgetbv1 xsavec cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local wbnoivd dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req avx512vbm1 umip pku ospke avx512_vbm1 qfni vaes vpclmulqdq avx512_vnni avx512_bitalg tme avx512_vpopcntdq 1a57 rdpid md_clear pconfig flush_l1d arch_capabilities

/proc/cpuinfo cache data
cache size : 58368 KB

(Continued on next page)
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Platform Notes (Continued)

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 2 nodes (0-1)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27
  28 29 30 31 32 33 34 35 36 37
  node 0 size: 1031742 MB
  node 0 free: 1030578 MB
  node 1 cpus: 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62
  63 64 65 66 67 68 69 70 71 72 73 74 75
  node 1 size: 1032178 MB
  node 1 free: 1028223 MB
  node distances:
    node 0 1
    0: 10 20
    1: 20 10

From /proc/meminfo
  MemTotal: 2113454812 kB
  HugePages_Total: 0
  Hugepagesize: 2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release*/etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15-SP2"
    VERSION_ID="15.2"
    PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
  Linux install 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
  x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store

(Continued on next page)
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Platform Notes (Continued)

CVE-2017-5753 (Spectre variant 1):
Bypass disabled via prctl and seccomp
Mitigation: usercopy/swapgs barriers and __user pointer sanitization

CVE-2017-5715 (Spectre variant 2):
Mitigation: Enhanced IBRS, IBPB:
conditional, RSB filling

CVE-2020-0543 (Special Register Buffer Data Sampling):
Not affected

CVE-2019-11135 (TSX Asynchronous Abort):
Not affected

run-level 3 Jul 28 10:30

SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda2 btrfs 222G 18G 203G 9% /home

From /sys/devices/virtual/dmi/id
Vendor: Cisco Systems Inc
Product: UCSC-C240-M6SX
Serial: WZP24440K0A

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200

BIOS:
BIOS Vendor: Cisco Systems, Inc.
BIOS Version: C240M6.4.2.1c.10.0723211453
BIOS Date: 07/23/2021
BIOS Revision: 5.22

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
| C | 619.lbm_s(base) 638.imagick_s(base) 644.nab_s(base) |
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================

(Continued on next page)
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Compiler Version Notes (Continued)

==============================================================================
| C++, C, Fortran | 607.cactuBSSN_s(base) |
| Intel(R) C++ Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000 |
| Copyright (C) 1985-2020 Intel Corporation. All rights reserved. |
| Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000 |
| Copyright (C) 1985-2020 Intel Corporation. All rights reserved. |
| Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000 |
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Base Compiler Invocation

C benchmarks:
  icc

Fortran benchmarks:
  ifort

Benchmarks using both Fortran and C:
  ifort icc

Benchmarks using Fortran, C, and C++:
  icpc icc ifort
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**SPECspeed®2017_fp_base = 228**

**SPECspeed®2017_fp_peak = Not Run**

#### Base Portability Flags

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#### Base Optimization Flags

**C benchmarks:**

- \(-m64 -std=c11 -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP -mbranches-within-32B-boundaries\)

**Fortran benchmarks:**

- \(-m64 -Wl,-z,muldefs -DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -nostandard-realloc-lhs -mbranches-within-32B-boundaries -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc\)

**Benchmarks using both Fortran and C:**

- \(-m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP -mbranches-within-32B-boundaries -nostandard-realloc-lhs -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc\)

**Benchmarks using Fortran, C, and C++:**

- \(-m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP -mbranches-within-32B-boundaries -nostandard-realloc-lhs -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc\)

The flags files that were used to format this result can be browsed at:

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Software Availability: Dec-2020

You can also download the XML flags sources by saving the following links:


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