Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6334, 3.60GHz)

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<td>32</td>
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</tr>
</tbody>
</table>

**Hardware**

- **CPU Name:** Intel Xeon Gold 6334
- **Max MHz:** 3700
- **Nominal:** 3600
- **Enabled:** 16 cores, 2 chips, 2 threads/core
- **Orderable:** 1.2 Chips
- **Cache L1:** 32 KB I + 48 KB D on chip per core
- **L2:** 1.25 MB I+D on chip per core
- **L3:** 18 MB I+D on chip per chip
- **Memory:** 2 TB (32 x 64 GB 2Rx4 PC4-3200AA-R)
- **Storage:** 1 x 480 GB SATA SSD
- **Other:** None

**Software**

- **OS:** SUSE Linux Enterprise Server 15 SP2
- **Compiler:** C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux;
  Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux;
  C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux
- **Parallel:** No
- **Firmware:** Version 4.2.1 released Jun-2021
- **File System:** btrfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 32/64-bit
- **Other:** jemalloc memory allocator V5.0.1
- **Power Management:** BIOS and OS set to prefer performance at the cost of additional power usage
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6334, 3.60GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jul-2021
Hardware Availability: Jun-2021
Software Availability: Mar-2021

Results Table

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"
MALLOC_CONF = "retain:true"

General Notes
Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numaclt i.e.:
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6334, 3.60GHz)  
SPEC CPU®2017 Integer Rate Result

SPECrater®2017_int_base = 145
SPECrater®2017_int_peak = 149

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<th>9019</th>
<th>Test Date:</th>
<th>Jul-2021</th>
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<td>Cisco Systems</td>
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<td>Cisco Systems</td>
<td>Software Availability:</td>
<td>Mar-2021</td>
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</tbody>
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General Notes (Continued)

numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
UPI Link Enablement set to 1
UPI Power Management set to Enabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDDC Sparing set to Disabled
Patrol Scrub set to Disabled
Energy Efficient Turbo set to Enabled
Processor C6 Report set to Enabled
Processor C1E set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acfc64d running on install Wed Jul 14 01:39:14 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
  model name : Intel(R) Xeon(R) Gold 6334 CPU @ 3.60GHz
  2 "physical id"s (chips)
  32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 8
  siblings : 16
  physical 0: cores 0 1 2 3 4 5 6 7
  physical 1: cores 0 1 2 3 4 5 6 7

(Continued on next page)
# SPEC CPU®2017 Integer Rate Result

## Cisco Systems

Cisco UCS B200 M6 (Intel Xeon Gold 6334, 3.60GHz)

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### Platform Notes (Continued)

From `lscpu` from `util-linux 2.33.1`:

- **Architecture:** x86_64
- **CPU op-mode(s):** 32-bit, 64-bit
- **Byte Order:** Little Endian
- **Address sizes:** 46 bits physical, 57 bits virtual
- **CPU(s):** 32
- **On-line CPU(s) list:** 0-31
- **Thread(s) per core:** 2
- **Core(s) per socket:** 8
- **Socket(s):** 2
- **NUMA node(s):** 4
- **Vendor ID:** GenuineIntel
- **CPU family:** 6
- **Model:** 106
- **Model name:** Intel(R) Xeon(R) Gold 6334 CPU @ 3.60GHz
- **Stepping:** 6
- **CPU MHz:** 2682.755
- **CPU max MHz:** 3700.0000
- **CPU min MHz:** 800.0000
- **BogoMIPS:** 7200.00
- **Virtualization:** VT-x
- **L1d cache:** 48K
- **L1i cache:** 32K
- **L2 cache:** 1280K
- **L3 cache:** 18432K
- **NUMA node0 CPU(s):** 0-3,16-19
- **NUMA node1 CPU(s):** 4-7,20-23
- **NUMA node2 CPU(s):** 8-11,24-27
- **NUMA node3 CPU(s):** 12-15,28-31
- **Flags:** fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
  pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
  lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
  aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
  xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tscdeadline_timer aes xsave
  avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invpcid_single ssbd
  mba ibrs ibpb ibrsenhanced tpr_shadow vmni flexpriority ept vpid ept_ad
  fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm rdt_a avx512f
  avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha ni
  avx512bw avx512vl xsaveopt xsavexstate x86save xstate lg鼋浮/gx vmm United States
  cqm_llc cgq_occum llc cgq_mbb total
  cgq_mbb_local wbinvd dtherm ida arat pln pts hwp hwp_act_window hwp epp
  hwp_pkg_req avx512vbmi umip pku ospke avx512_vbmi2 gfn i vaes vpcmldq avg avx512_vnni
  avx512_bitalg tme avx512_vpopcntdq la57 rdpid md_clear pconfi flush_lld
  arch_capabilities

/proc/cpuinfo cache data
- **cache size:** 18432 KB

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6334, 3.60GHz)

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CPU2017 License: 9019
Test Sponsor: Cisco Systems
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Test Date: Jul-2021
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Platform Notes (Continued)

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
   available: 4 nodes (0-3)
   node 0 cpus: 0 1 2 3 16 17 18 19
   node 0 size: 515495 MB
   node 0 free: 515209 MB
   node 1 cpus: 4 5 6 7 20 21 22 23
   node 1 size: 516093 MB
   node 1 free: 515823 MB
   node 2 cpus: 8 9 10 11 24 25 26 27
   node 2 size: 516093 MB
   node 2 free: 515867 MB
   node 3 cpus: 12 13 14 15 28 29 30 31
   node 3 size: 516090 MB
   node 3 free: 515793 MB
   node distances:
   node   0   1   2   3
         0: 10 11 20 20
         1: 11 10 20 20
         2: 20 20 10 11
         3: 20 20 11 10

From /proc/meminfo
   MemTotal: 2113303288 kB
   HugePages_Total: 0
   Hugepagesize: 2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release*/etc/*version*
   os-release:
     NAME="SLES"
     VERSION="15-SP2"
     VERSION_ID="15.2"
     PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
     ID="sles"
     ID_LIKE="suse"
     ANSI_COLOR="0;32"
     CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
   Linux install 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
   x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6334, 3.60GHz)

**SPEC CPU®2017 Integer Rate Result**

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**CPU2017 License:** 9019  
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**Test Date:** Jul-2021  
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**Platform Notes (Continued)**

- **CVE-2018-12207 (iTLB Multihit):** Not affected  
- **CVE-2018-3620 (L1 Terminal Fault):** Not affected  
- **Microarchitectural Data Sampling:** Not affected  
- **CVE-2017-5754 (Meltdown):** Not affected  
- **CVE-2018-3639 (Speculative Store Bypass):** Mitigation: Speculative Store Bypass disabled via prctl and seccomp  
- **CVE-2017-5753 (Spectre variant 1):** Mitigation: usercopy/swaps barriers and __user pointer sanitation  
- **CVE-2017-5715 (Spectre variant 2):** Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling  
- **CVE-2020-0543 (Special Register Buffer Data Sampling):** Not affected  
- **CVE-2019-11135 (TSX Asynchronous Abort):** Not affected

---

**run-level 3 Jul 14 01:35**

**SPEC is set to:** /home/cpu2017  
**Filesystem** | **Type** | **Size** | **Used** | **Avail** | **Use%** | **Mounted on**
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<td>/dev/sda4</td>
<td>btrfs</td>
<td>445G</td>
<td>16G</td>
<td>428G</td>
<td>4%</td>
<td>/home</td>
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</tbody>
</table>

**From /sys/devices/virtual/dmi/id**

| **Vendor:** Cisco Systems Inc  
| **Product:** UCSB-B200-M6  
| **Serial:** FCH24097576

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

**Memory:**

32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200

**BIOS:**

| **BIOS Vendor:** Cisco Systems, Inc.  
| **BIOS Version:** B200M6.4.2.1.41.0625210158  
| **BIOS Date:** 06/25/2021  
| **BIOS Revision:** 5.22

(End of data from sysinfo program)

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**Compiler Version Notes**

```
C | 500.perlbench_r(peak) 557.xz_r(peak)
```

(Continued on next page)
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Cisco UCS B200 M6 (Intel Xeon Gold 6334, 3.60GHz)

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CPU2017 License: 9019
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Tested by: Cisco Systems

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<th>548.exchange2_r(base, peak)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000</td>
<td></td>
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<tr>
<td>Copyright (C) 1985-2020 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
</tbody>
</table>

Base Compiler Invocation

C benchmarks:
icx

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6334, 3.60GHz)

SPECrete®2017_int_base = 145
SPECrete®2017_int_peak = 149

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jul-2021
Hardware Availability: Jun-2021
Software Availability: Mar-2021

Base Compiler Invocation (Continued)

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

C++ benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

Fortran benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-auto -mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin

(Continued on next page)
Cisco Systems
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Base Optimization Flags (Continued)

Fortran benchmarks (continued):
-1qkmalloc

Peak Compiler Invocation

C benchmarks (except as noted below):
icx
500.perlbench_r: icc
557.xz_r: icc
C++ benchmarks:
icpx
Fortran benchmarks:
ifort

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:
500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)
-xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-strict-overflow
-mbraches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6334, 3.60GHz)

SPEC CPU®2017 Integer Rate Result
Copyright 2017-2021 Standard Performance Evaluation Corporation

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jul-2021
Hardware Availability: Jun-2021
Software Availability: Mar-2021

SPECrate®2017_int_base = 145
SPECrate®2017_int_peak = 149

Peak Optimization Flags (Continued)

500.perlbench_r (continued):
-1qkmalloc

502.gcc_r: -m32
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/ia32_lin
-std=gnu89 -Wl,-z,muldefs -fprofile-generate(pass 1)
-fprofile-use=default.profdatal -xCORE-AVX512 -flto
-Ofast(pass 1) -O3 -ffast-math -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/usr/local/jemalloc32-5.0.1/lib -ljemalloc

505.mcf_r: basepeak = yes

525.x264_r: -w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -flto
-O3 -ffast-math -qopt-mem-layout-trans=4 -fno-alias
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-1qkmalloc

557.xz_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-1qkmalloc

C++ benchmarks:

520.omnetpp_r: basepeak = yes

523.xalancbmk_r: basepeak = yes

531.deepsjeng_r: basepeak = yes

541.leela_r: basepeak = yes

Fortran benchmarks:

548.exchange2_r: basepeak = yes

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.0-ICX-revF.xml
## SPEC CPU®2017 Integer Rate Result

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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