Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6354, 3.00GHz)

SPECrate®2017_fp_base = 320
SPECrate®2017_fp_peak = Not Run

<table>
<thead>
<tr>
<th>Software</th>
<th>Hardware</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS: SUSE Linux Enterprise Server 15 SP2 5.3.18-22-default</td>
<td>CPU Name: Intel Xeon Gold 6354</td>
</tr>
<tr>
<td>Compiler: C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux; Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux;</td>
<td>Max MHz: 3600</td>
</tr>
<tr>
<td>Parallel: No</td>
<td>Nominal: 3000</td>
</tr>
<tr>
<td>Firmware: Version 4.2.1 released Jun-2021</td>
<td>Enabled: 36 cores, 2 chips, 2 threads/core</td>
</tr>
<tr>
<td>File System: btrfs</td>
<td>Orderable: 1,2 Chips</td>
</tr>
<tr>
<td>System State: Run level 3 (multi-user)</td>
<td>Cache L1: 32 KB I + 48 KB D on chip per core</td>
</tr>
<tr>
<td>Base Pointers: 64-bit</td>
<td>L2: 1.25 MB I+D on chip per core</td>
</tr>
<tr>
<td>Peak Pointers: Not Applicable</td>
<td>L3: 39 MB I+D on chip per chip</td>
</tr>
<tr>
<td>Other: jemalloc memory allocator V5.0.1</td>
<td>Other: None</td>
</tr>
<tr>
<td>Power Management: BIOS and OS set to prefer performance at the cost of additional power usage</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Copies</th>
<th>503.bwaves_r</th>
<th>72</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>507.cactuBSSN_r</td>
<td>72</td>
</tr>
<tr>
<td></td>
<td>508.namd_r</td>
<td>72</td>
</tr>
<tr>
<td></td>
<td>510.parest_r</td>
<td>72</td>
</tr>
<tr>
<td></td>
<td>511.povray_r</td>
<td>72</td>
</tr>
<tr>
<td></td>
<td>519.lbm_r</td>
<td>72</td>
</tr>
<tr>
<td></td>
<td>521.wrf_r</td>
<td>72</td>
</tr>
<tr>
<td></td>
<td>526.blender_r</td>
<td>72</td>
</tr>
<tr>
<td></td>
<td>527.cam4_r</td>
<td>72</td>
</tr>
<tr>
<td></td>
<td>538.imagick_r</td>
<td>72</td>
</tr>
<tr>
<td></td>
<td>544.nab_r</td>
<td>72</td>
</tr>
<tr>
<td></td>
<td>549.fotonik3d_r</td>
<td>72</td>
</tr>
<tr>
<td></td>
<td>554.roms_r</td>
<td>72</td>
</tr>
</tbody>
</table>

Hardware
CPU Name: Intel Xeon Gold 6354
Max MHz: 3600
Nominal: 3000
Enabled: 36 cores, 2 chips, 2 threads/core
Orderable: 1,2 Chips
Cache L1: 32 KB I + 48 KB D on chip per core
L2: 1.25 MB I+D on chip per core
L3: 39 MB I+D on chip per chip
Other: None
Memory: 2 TB (32 x 64 GB 2Rx4 PC4-3200V-R)
Storage: 1 x 480 GB SATA SSD
Other: None
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6354, 3.00GHz)

CPUs: 16

SPECraté\textsuperscript{2017} fp\_base = 320
SPECraté\textsuperscript{2017} fp\_peak = Not Run

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>72</td>
<td>1036</td>
<td>697</td>
<td>1038</td>
<td>696</td>
<td>1036</td>
<td>697</td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>72</td>
<td>223</td>
<td>408</td>
<td>225</td>
<td>405</td>
<td>223</td>
<td>408</td>
</tr>
<tr>
<td>508.namd_r</td>
<td>72</td>
<td>304</td>
<td>225</td>
<td>307</td>
<td>223</td>
<td>304</td>
<td>225</td>
</tr>
<tr>
<td>510.parest_r</td>
<td>72</td>
<td>1011</td>
<td>186</td>
<td>1014</td>
<td>186</td>
<td>1012</td>
<td>186</td>
</tr>
<tr>
<td>511.povray_r</td>
<td>72</td>
<td>510</td>
<td>330</td>
<td>509</td>
<td>331</td>
<td>509</td>
<td>330</td>
</tr>
<tr>
<td>519.lbm_r</td>
<td>72</td>
<td>298</td>
<td>255</td>
<td>298</td>
<td>255</td>
<td>298</td>
<td>255</td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>72</td>
<td>521</td>
<td>310</td>
<td>549</td>
<td>294</td>
<td>512</td>
<td>315</td>
</tr>
<tr>
<td>526.blender_r</td>
<td>72</td>
<td>363</td>
<td>302</td>
<td>363</td>
<td>302</td>
<td>363</td>
<td>302</td>
</tr>
<tr>
<td>527.cam4_r</td>
<td>72</td>
<td>399</td>
<td>315</td>
<td>402</td>
<td>313</td>
<td>401</td>
<td>314</td>
</tr>
<tr>
<td>538.imagick_r</td>
<td>72</td>
<td>225</td>
<td>797</td>
<td>258</td>
<td>694</td>
<td>223</td>
<td>802</td>
</tr>
<tr>
<td>544.nab_r</td>
<td>72</td>
<td>239</td>
<td>507</td>
<td>243</td>
<td>498</td>
<td>240</td>
<td>504</td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
<td>72</td>
<td>1310</td>
<td>214</td>
<td>1305</td>
<td>215</td>
<td>1302</td>
<td>215</td>
</tr>
<tr>
<td>554.roms_r</td>
<td>72</td>
<td>781</td>
<td>146</td>
<td>772</td>
<td>148</td>
<td>773</td>
<td>148</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD\_LIBRARY\_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOC\_CONF = "retain:true"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6354, 3.00GHz)

SPECRate®2017_fp_base = 320
SPECRate®2017_fp_peak = Not Run

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
<th>Test Date:</th>
<th>Jul-2021</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
<td>Hardware Availability:</td>
<td>Jun-2021</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
<td>Software Availability:</td>
<td>Mar-2021</td>
</tr>
</tbody>
</table>

General Notes (Continued)

```bash
core 3>   /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
    numactl --interleave=all runcpu <etc>
```

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.


Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
UPI Link Enablement set to 1
UPI Power Management set to Enabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDC Sparing set to Disabled
Patrol Scrub set to Disabled
Energy Efficient Turbo set to Enabled
Processor C6 Report set to Enabled
Processor C1E set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec915b55891ef0e16acaf64d
running on install Thu Jul 8 19:43:10 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
```
model name : Intel(R) Xeon(R) Gold 6354 CPU @ 3.00GHz
   2 "physical id"'s (chips)
   72 "processors"
core, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 18
siblings : 36
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
```

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6354, 3.00GHz)

SPEC CPU®2017 Floating Point Rate Result

SPECrate®2017_fp_base = 320
SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Jul-2021
Hardware Availability: Jun-2021
Tested by: Cisco Systems
Software Availability: Mar-2021

Platform Notes (Continued)

physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17

From lscpu from util-linux 2.33.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 72
On-line CPU(s) list: 0-71
Thread(s) per core: 2
Core(s) per socket: 18
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Gold 6354 CPU @ 3.00GHz
Stepping: 6
CPU MHz: 2751.640
CPU max MHz: 3600.0000
CPU min MHz: 800.0000
BogoMIPS: 6000.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 39936K
NUMA node0 CPU(s): 0-8,36-44
NUMA node1 CPU(s): 9-17,45-53
NUMA node2 CPU(s): 18-26,54-62
NUMA node3 CPU(s): 27-35,63-71
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdelgb rdtsc
lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aerfmperef pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtrr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invpcid_single ssbd
mbs ibrs ibpb stibp ibrs_enhanced tpr_shadow vmmi flexpriority ept vpid ept_ad
fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm rdt_a avx512f
avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cdsha ni
avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbb_total
cqm_mbb_local wbinvd dtherm ida arat pln pts hwp hwp_act_window hwp_epp
hwp_pkg_req avx512vmbmi umip pku ospke avx512vmbmi gfn i vaes vpcmulongq avx512_vnni
avx512_bitalg tme avx512_vpopcntdq 1a57 rdpid md_clear pconfig flush_l1d
arch_capabilities

/proc/cpuinfo cache data

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6354, 3.00GHz)

<table>
<thead>
<tr>
<th>CPU2017 License</th>
<th>Test Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>9019</td>
<td>Jul-2021</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Test Sponsor</th>
<th>Hardware Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cisco Systems</td>
<td>Jun-2021</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Tested by</th>
<th>Software Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cisco Systems</td>
<td>Mar-2021</td>
</tr>
</tbody>
</table>

SPECrater®2017_fp_base = 320
SPECrater®2017_fp_peak = Not Run

cache size : 39936 KB

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 4 5 6 7 8 36 37 38 39 40 41 42 43 44
node 0 size: 515527 MB
node 0 free: 515217 MB
node 1 cpus: 9 10 11 12 13 14 15 16 17 45 46 47 48 49 50 51 52 53
node 1 size: 516091 MB
node 1 free: 515753 MB
node 2 cpus: 18 19 20 21 22 23 24 25 26 54 55 56 57 58 59 60 61 62
node 2 size: 516091 MB
node 2 free: 515838 MB
node 3 cpus: 27 28 29 30 31 32 33 34 35 63 64 65 66 67 68 69 70 71
node 3 size: 516054 MB
node 3 free: 515763 MB
node distances:
node 0 1 2 3
0: 10 11 20 20
1: 11 10 20 20
2: 20 20 10 11
3: 20 20 11 10

From /proc/meminfo
MemTotal: 2113294356 kB
HugePages_Total: 0
Hugepagesize: 2048 kB
/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*

os-release:
NAME="SLES"
VERSION="15-SP2"
VERSION_ID="15.2"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
Linux install 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64 x86_64 x86_64 GNU/Linux

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6354, 3.00GHz)

SPECraten®2017_fp_base = 320
SPECraten®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jul-2021
Hardware Availability: Jun-2021
Software Availability: Mar-2021

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs barriers and __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Jul 8 19:40

SPECraten is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda4 btrfs 445G 16G 428G 4% /home

From /sys/devices/virtual/dmi/id
Vendor: Cisco Systems Inc
Product: UCSB-B200-M6
Serial: FCH24097576

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBOIS" standard.

Memory:
32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200

BIOS:
BIOS Vendor: Cisco Systems, Inc.
BIOS Version: B200M6.4.2.1.41.0625210158
BIOS Date: 06/25/2021
BIOS Revision: 5.22

(End of data from sysinfo program)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6354, 3.00GHz)

SPECrate®2017_fp_base = 320
SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Jul-2021
Tested by: Cisco Systems
Hardware Availability: Jun-2021
Software Availability: Mar-2021

Compiler Version Notes
==============================================================================
C                                           | 519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

C++                                         | 508.namd_r(base) 510.parest_r(base)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

C++, C                                       | 511.povray_r(base) 526.blender_r(base)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

C++, C, Fortran                               | 507.cactuBSSN_r(base)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Fortran                                      | 503.bwaves_r(base) 549.fotonik3d_r(base) 554.roms_r(base)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6354, 3.00GHz)

SPECrater®2017_fp_base = 320
SPECrater®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Jul-2021
Hardware Availability: Jun-2021
Software Availability: Mar-2021

Compiler Version Notes (Continued)

==============================================================================
Fortran, C      | 521.wrf_r(base) 527.cam4_r(base)
------------------------------------------------------------------------------

Intel (R) Fortran Intel (R) 64 Compiler Classic for applications running on
Intel (R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel (R) oneAPI DPC++/C++ Compiler for applications running on Intel (R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================

Base Compiler Invocation

C benchmarks:
icx
C++ benchmarks:
icpx
Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icx

Benchmarks using both C and C++:
icpx icx

Benchmarks using Fortran, C, and C++:
icpx icx ifort

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsinged-char

(Continued on next page)
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6354, 3.00GHz)

| CPU2017 License:          | 9019 |
| Test Sponsor:             | Cisco Systems |
| Tested by:                | Cisco Systems |
| Test Date:                | Jul-2021 |
| Hardware Availability:    | Jun-2021 |
| Software Availability:    | Mar-2021 |

SPECrater®2017_fp_base = 320
SPECrater®2017_fp_peak = Not Run

### Base Portability Flags (Continued)

| 527.cam4_r: | -DSPEC_LP64 -DSPEC_CASE_FLAG |
| 538.imagick_r: | -DSPEC_LP64 |
| 544.nab_r: | -DSPEC_LP64 |
| 549.fotonik3d_r: | -DSPEC_LP64 |
| 554.roms_r: | -DSPEC_LP64 |

### Base Optimization Flags

**C benchmarks:**
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

**C++ benchmarks:**
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

**Fortran benchmarks:**
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
-qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

**Benchmarks using both Fortran and C:**
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

**Benchmarks using both C and C++:**
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

**Benchmarks using Fortran, C, and C++:**
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
Cisco Systems
Cisco UCS B200 M6 (Intel Xeon Gold 6354, 3.00GHz)

SPECrate®2017_fp_base = 320
SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jul-2021
Hardware Availability: Jun-2021
Software Availability: Mar-2021

Base Optimization Flags (Continued)

Benchmarks using Fortran, C, and C++ (continued):
- flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3
- no-prec-div -qopt-prefetch -ffinite-math-only
- qopt-multiple-gather-scatter-by-shuffles
- mbranches-within-32B-boundaries -nostandard-realloc-lhs
- align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.0-ICX-revF.xml

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.8 on 2021-07-08 19:43:10-0400.
Originally published on 2021-08-04.