## Cisco Systems

Cisco UCS C240 M6 (Intel Xeon Gold 5320, 2.20GHz)

<table>
<thead>
<tr>
<th>Software</th>
<th>Hardware</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS: SUSE Linux Enterprise Server 15 SP2 5.3.18-22-default</td>
<td>CPU Name: Intel Xeon Gold 5320 Max MHz: 3400 Nominal: 2200</td>
</tr>
<tr>
<td>Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux; Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux; C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux</td>
<td>Enabled: 52 cores, 2 chips, 2 threads/core Orderable: 1.2 Chips</td>
</tr>
<tr>
<td>Firmware: Version 4.2.1c released Jul-2021</td>
<td>Cache L1: 32 KB I + 48 KB D on chip per core</td>
</tr>
<tr>
<td>File System: btrfs</td>
<td>L2: 1.25 MB I+D on chip per core</td>
</tr>
<tr>
<td>System State: Run level 3 (multi-user)</td>
<td>L3: 39 MB I+D on chip per chip</td>
</tr>
<tr>
<td>Base Pointers: 64-bit</td>
<td>Other: None</td>
</tr>
<tr>
<td>Peak Pointers: 32/64-bit</td>
<td>Memory: 2 TB (32 x 64 GB 2Rx4 PC4-3200AA-R, running at 2933)</td>
</tr>
<tr>
<td>Other: jemalloc memory allocator V5.0.1</td>
<td>Storage: 1 x 300 GB 15K SAS HDD</td>
</tr>
<tr>
<td>Power Management: BIOS and OS set to prefer performance at the cost of additional power usage</td>
<td>Other: None</td>
</tr>
</tbody>
</table>

**Test Sponsor:** Cisco Systems  
**Test Date:** Jul-2021  
**Hardware Availability:** Jun-2021  
**Software Availability:** Mar-2021

---

### SPEC CPU®2017 Integer Rate Result

**SPECrate®2017_int_peak = 372**  
**SPECrate®2017_int_base = 359**

<table>
<thead>
<tr>
<th>Test Date</th>
<th>Hardware Availability</th>
<th>Software Availability</th>
<th>Tested by</th>
<th>Test Sponsor</th>
<th>CPU2017 License</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Application</th>
<th>Copies</th>
<th>SPECrate®2017_int_base</th>
<th>SPECrate®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>104</td>
<td><em>(247)</em></td>
<td><em>(290)</em></td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>104</td>
<td><em>(343)</em></td>
<td><em>(372)</em></td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>104</td>
<td><em>(454)</em></td>
<td><em>(480)</em></td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>104</td>
<td><em>(221)</em></td>
<td><em>(273)</em></td>
</tr>
<tr>
<td>523.xalanchmk_r</td>
<td>104</td>
<td><em>(608)</em></td>
<td><em>(738)</em></td>
</tr>
<tr>
<td>525.x264_r</td>
<td>104</td>
<td><em>(742)</em></td>
<td><em>(774)</em></td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>104</td>
<td><em>(203)</em></td>
<td><em>(203)</em></td>
</tr>
<tr>
<td>541.leela_r</td>
<td>104</td>
<td><em>(268)</em></td>
<td><em>(268)</em></td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>104</td>
<td><em>(780)</em></td>
<td><em>(780)</em></td>
</tr>
<tr>
<td>557.xz_r</td>
<td>104</td>
<td><em>(510)</em></td>
<td><em>(510)</em></td>
</tr>
</tbody>
</table>

---

**Tested by:** Cisco Systems  
**CPU2017 License:** 9019
## Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 5320, 2.20GHz)

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

---

### SPEC CPU 2017 Integer Rate Result

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>104</td>
<td>671</td>
<td>247</td>
<td>671</td>
<td>247</td>
<td>671</td>
<td>247</td>
<td>104</td>
<td>671</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>104</td>
<td>500</td>
<td>294</td>
<td>503</td>
<td>293</td>
<td>500</td>
<td>294</td>
<td>104</td>
<td>500</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>104</td>
<td>277</td>
<td>606</td>
<td>275</td>
<td>611</td>
<td>276</td>
<td>608</td>
<td>104</td>
<td>277</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>104</td>
<td>616</td>
<td>221</td>
<td>616</td>
<td>221</td>
<td>617</td>
<td>221</td>
<td>104</td>
<td>616</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>104</td>
<td>242</td>
<td>454</td>
<td>242</td>
<td>454</td>
<td>242</td>
<td>453</td>
<td>104</td>
<td>242</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>104</td>
<td>245</td>
<td>742</td>
<td>245</td>
<td>742</td>
<td>245</td>
<td>742</td>
<td>104</td>
<td>245</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>104</td>
<td>437</td>
<td>273</td>
<td>437</td>
<td>273</td>
<td>437</td>
<td>273</td>
<td>104</td>
<td>437</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>104</td>
<td>642</td>
<td>268</td>
<td>641</td>
<td>269</td>
<td>642</td>
<td>268</td>
<td>104</td>
<td>642</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>104</td>
<td>370</td>
<td>736</td>
<td>369</td>
<td>738</td>
<td>369</td>
<td>738</td>
<td>104</td>
<td>370</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>104</td>
<td>554</td>
<td>203</td>
<td>555</td>
<td>202</td>
<td>554</td>
<td>203</td>
<td>104</td>
<td>554</td>
</tr>
</tbody>
</table>

**SPECrate®2017_int_base = 359**  
**SPECrate®2017_int_peak = 372**

---

### Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>104</td>
<td>671</td>
<td>247</td>
<td>671</td>
<td>247</td>
<td>671</td>
<td>247</td>
<td>104</td>
<td>671</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>104</td>
<td>500</td>
<td>294</td>
<td>503</td>
<td>293</td>
<td>500</td>
<td>294</td>
<td>104</td>
<td>500</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>104</td>
<td>277</td>
<td>606</td>
<td>275</td>
<td>611</td>
<td>276</td>
<td>608</td>
<td>104</td>
<td>277</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>104</td>
<td>616</td>
<td>221</td>
<td>616</td>
<td>221</td>
<td>617</td>
<td>221</td>
<td>104</td>
<td>616</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>104</td>
<td>242</td>
<td>454</td>
<td>242</td>
<td>454</td>
<td>242</td>
<td>453</td>
<td>104</td>
<td>242</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>104</td>
<td>245</td>
<td>742</td>
<td>245</td>
<td>742</td>
<td>245</td>
<td>742</td>
<td>104</td>
<td>245</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>104</td>
<td>437</td>
<td>273</td>
<td>437</td>
<td>273</td>
<td>437</td>
<td>273</td>
<td>104</td>
<td>437</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>104</td>
<td>642</td>
<td>268</td>
<td>641</td>
<td>269</td>
<td>642</td>
<td>268</td>
<td>104</td>
<td>642</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>104</td>
<td>370</td>
<td>736</td>
<td>369</td>
<td>738</td>
<td>369</td>
<td>738</td>
<td>104</td>
<td>370</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>104</td>
<td>554</td>
<td>203</td>
<td>555</td>
<td>202</td>
<td>554</td>
<td>203</td>
<td>104</td>
<td>554</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:

- `LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"
- `MALLOCONF = "retain: true"

### General Notes

Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM  
Memory using openSUSE Leap 15.2  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation  
Filesystem page cache synced and cleared with:

```
sync; echo 3 > /proc/sys/vm/drop_caches
```

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 5320, 2.20GHz)

SPEC CPU®2017 Integer Rate Result

SPECrate®2017_int_base = 359
SPECrate®2017_int_peak = 372

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jul-2021
Hardware Availability: Jun-2021
Software Availability: Mar-2021

General Notes (Continued)

runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.


Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
UPI Link Enablement set to 1
UPI Power Management set to Enabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDCS Sparing set to Disabled
Patrol Scrub set to Disabled
Energy Efficient Turbo set to Enabled
Processor C6 Report set to Enabled
Processor C1E set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16aacafrica64d
running on install Fri Jul 16 19:49:26 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 5320 CPU @ 2.20GHz
  2 "physical id"s (chips)
  104 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 26
siblings : 52
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25

(Continued on next page)
**Platform Notes (Continued)**

physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25

From lscpu from util-linux 2.33.1:

Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 104
On-line CPU(s) list: 0-103
Thread(s) per core: 2
Core(s) per socket: 26
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Gold 5320 CPU @ 2.20GHz
Stepping: 6
CPU MHz: 3044.949
CPU max MHz: 3400.0000
CPU min MHz: 800.0000
BogoMIPS: 4400.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 39936K
NUMA node0 CPU(s): 0-12,52-64
NUMA node1 CPU(s): 13-25,65-77
NUMA node2 CPU(s): 26-38,78-90
NUMA node3 CPU(s): 39-51,91-103
Flags: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xapic nondis interrupt ibpb mce p LVmxpages big_pages diltdtl3_discount tsc_validate lock_国籍 lock_国籍 tsc tsc_ADAPT

(Continued on next page)
Platform Notes (Continued)

/proc/cpuinfo cache data
  cache size : 39936 KB

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
  available: 4 nodes (0-3)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 52 53 54 55 56 57 58 59 60 61 62 63 64
  node 0 size: 515682 MB
  node 0 free: 515258 MB
  node 1 cpus: 13 14 15 16 17 18 19 20 21 22 23 24 25 65 66 67 68 69 70 71 72 73 74 75 76
  node 1 size: 516089 MB
  node 1 free: 515612 MB
  node 2 cpus: 26 27 28 29 30 31 32 33 34 35 36 37 38 78 79 80 81 82 83 84 85 86 87 88 89
  node 2 size: 516055 MB
  node 2 free: 515618 MB
  node 3 cpus: 39 40 41 42 43 44 45 46 47 48 49 50 51 91 92 93 94 95 96 97 98 99 100 101
  node 3 size: 516085 MB
  node 3 free: 515805 MB
  node distances:
  node   0   1   2   3
  0:  10  11  20  20
  1:  11  10  20  20
  2:  20  20  10  11
  3:  20  20  11  10

From /proc/meminfo
  MemTotal:       2113447492 kB
  HugePages_Total:       0
  Hugepagesize:       2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15-SP2"
    VERSION_ID="15.2"
    PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15:sp2"

(Continued on next page)
Platform Notes (Continued)

uname -a:
Linux install 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit):                        Not affected
CVE-2018-3620 (L1 Terminal Fault):                     Not affected
Microarchitectural Data Sampling:                      Not affected
CVE-2017-5754 (Meltdown):                              Not affected
CVE-2018-3639 (Speculative Store Bypass):              Mitigation: Speculative Store
Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1):                     Mitigation: usercopy/swapgs barriers and __user pointer
sanitization
CVE-2017-5715 (Spectre variant 2):                     Mitigation: Enhanced IBRS, IBPB:
conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort):               Not affected

run-level 3 Jul 16 19:47

SPEC is set to: /home/cpu2017
Filesystem     Type   Size  Used Avail Use% Mounted on
/dev/sdc2      btrfs  277G  26G  250G 10% /home

From /sys/devices/virtual/dmi/id
Vendor:         Cisco Systems Inc
Product:        UCSC-C240-M6SX
Serial:         WZP244208SJ

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you
interpret this section. The 'dmidecode' program reads system data which is "intended to
allow hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200, configured at 2933

BIOS:
  BIOS Vendor:    Cisco Systems, Inc.
  BIOS Version:   C240M6.4.2.1c.1.0701210708
  BIOS Date:      07/01/2021
  BIOS Revision:  5.22

(End of data from sysinfo program)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 5320, 2.20GHz)

SPECrate®2017_int_base = 359
SPECrate®2017_int_peak = 372

CPU2017 License: 9019
Test Date: Jul-2021
Test Sponsor: Cisco Systems
Hardware Availability: Jun-2021
Tested by: Cisco Systems
Software Availability: Mar-2021

Compiler Version Notes

==============================================================================
C       | 500.perlbench_r(peak) 557.xz_r(peak)
-----------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
-----------------------------------------------------------------------------

==============================================================================
C       | 502.gcc_r(peak)
-----------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
-----------------------------------------------------------------------------

==============================================================================
C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
| 525.x264_r(base, peak) 557.xz_r(base)
-----------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
-----------------------------------------------------------------------------

==============================================================================
C       | 500.perlbench_r(peak) 557.xz_r(peak)
-----------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
-----------------------------------------------------------------------------

==============================================================================
C       | 502.gcc_r(peak)
-----------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
-----------------------------------------------------------------------------

==============================================================================
C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
| 525.x264_r(base, peak) 557.xz_r(base)
-----------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 5320, 2.20GHz)

Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 5320, 2.20GHz)

SPECrate®2017_int_base = 359
SPECrate®2017_int_peak = 372

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jul-2021
Hardware Availability: Jun-2021
Software Availability: Mar-2021

Compiler Version Notes (Continued)

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

--------------------------------------------------------------------------------

C       | 500.perlbench_r(peak) 557.xz_r(peak)
--------------------------------------------------------------------------------

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
--------------------------------------------------------------------------------

C       | 502.gcc_r(peak)
--------------------------------------------------------------------------------

Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
--------------------------------------------------------------------------------

C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
| 525.x264_r(base, peak) 557.xz_r(base)
--------------------------------------------------------------------------------

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
--------------------------------------------------------------------------------

C++     | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base, peak)
| 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
--------------------------------------------------------------------------------

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
--------------------------------------------------------------------------------

Fortran | 548.exchange2_r(base, peak)
--------------------------------------------------------------------------------

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 5320, 2.20GHz)

SPECrate®2017_int_base = 359
SPECrate®2017_int_peak = 372

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jul-2021
Hardware Availability: Jun-2021
Software Availability: Mar-2021

Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

C++ benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

Fortran benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-auto -mbranches-within-32B-boundaries

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 5320, 2.20GHz)  

SPEC CPU®2017 Integer Rate Result
Copyright 2017-2021 Standard Performance Evaluation Corporation

SPECrate®2017_int_base = 359
SPECrate®2017_int_peak = 372

Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 5320, 2.20GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jul-2021
Hardware Availability: Jun-2021
Software Availability: Mar-2021

Base Optimization Flags (Continued)
Fortran benchmarks (continued):
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

Peak Compiler Invocation
C benchmarks (except as noted below):
icx
500.perlbench_r: icc
557.xz_r: icc
C++ benchmarks:
icpx
Fortran benchmarks:
ifort

Peak Portability Flags
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags
C benchmarks:
500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)
-xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-strict-overflow
-mbranches-within-32B-boundaries

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 5320, 2.20GHz)

Peak Optimization Flags (Continued)

500.perlbench_r (continued):
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

502.gcc_r: -m32
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/ia32_lin
-std=gnu89 -Wl,-z,muldefs -fprofile-generate(pass1)
-fprofile-use=default.profdata(pass 2) -xCORE-AVX512 -flto
-Ofast(pass 1) -O3 -ffast-math -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/usr/local/jemalloc32-5.0.1/lib -ljemalloc

505.mcf_r: basepeak = yes

525.x264_r: -w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -flto
-O3 -ffast-math -qopt-mem-layout-trans=4 -fno-alias
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

C++ benchmarks:

520.omnetpp_r: basepeak = yes

Fortran benchmarks:

548.exchange2_r: basepeak = yes

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.0-ICX-revF.xml
## SPEC CPU®2017 Integer Rate Result

### Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 5320, 2.20GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base = 359</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_int_peak = 372</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CPU2017 License: 9019</th>
<th>Test Date: Jul-2021</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor: Cisco Systems</td>
<td>Hardware Availability: Jun-2021</td>
</tr>
<tr>
<td>Tested by: Cisco Systems</td>
<td>Software Availability: Mar-2021</td>
</tr>
</tbody>
</table>

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.8 on 2021-07-16 22:49:25-0400.
Report generated on 2021-08-04 18:22:05 by CPU2017 PDF formatter v6442.
Originally published on 2021-08-04.