Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 6348, 2.60GHz)

SPECrater®2017_int_base = 424
SPECrater®2017_int_peak = 439

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Hardware
CPU Name: Intel Xeon Gold 6348
Max MHz: 3500
Nominal: 2600
Enabled: 56 cores, 2 chips, 2 threads/core
Orderable: 1.2 Chips
Cache L1: 32 KB I + 48 KB D on chip per core
L2: 1.25 MB I+D on chip per core
L3: 42 MB I+D on chip per chip
Other: None
Memory: 2 TB (32 x 64 GB 2Rx4 PC4-3200AA-R)
Storage: 1 x 240 GB SATA SSD
Other: None

Software
OS: SUSE Linux Enterprise Server 15 SP2
5.3.18-22-default
Compiler: C/C++; Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux; Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux; C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux
Parallel: No
Firmware: Version 4.2.1c released Jul-2021
File System: btrfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 32/64-bit
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS and OS set to prefer performance at the cost of additional power usage

Test Date: Jul-2021
Hardware Availability: Jun-2021
Software Availability: Mar-2021
Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Base Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Peak Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Peak Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_int_base = 424</td>
<td></td>
<td></td>
<td></td>
<td>SPECrate®2017_int_peak = 439</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>500.perbench_r</td>
<td>112</td>
<td>606</td>
<td>294</td>
<td>610</td>
<td>292</td>
<td>612</td>
<td>291</td>
<td>112</td>
<td>526</td>
<td>339</td>
<td>526</td>
<td>339</td>
<td>524</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>112</td>
<td>479</td>
<td>331</td>
<td>481</td>
<td>330</td>
<td>478</td>
<td>332</td>
<td>112</td>
<td>404</td>
<td>392</td>
<td>404</td>
<td>392</td>
<td>403</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>112</td>
<td>262</td>
<td>692</td>
<td>261</td>
<td>694</td>
<td>260</td>
<td>697</td>
<td>112</td>
<td>262</td>
<td>692</td>
<td>261</td>
<td>694</td>
<td>260</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>112</td>
<td>599</td>
<td>245</td>
<td>600</td>
<td>245</td>
<td>599</td>
<td>245</td>
<td>112</td>
<td>599</td>
<td>245</td>
<td>599</td>
<td>245</td>
<td>599</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>112</td>
<td>225</td>
<td>526</td>
<td>226</td>
<td>524</td>
<td>225</td>
<td>526</td>
<td>112</td>
<td>225</td>
<td>526</td>
<td>225</td>
<td>526</td>
<td>225</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>112</td>
<td>224</td>
<td>875</td>
<td>226</td>
<td>868</td>
<td>224</td>
<td>876</td>
<td>112</td>
<td>213</td>
<td>922</td>
<td>214</td>
<td>917</td>
<td>214</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>112</td>
<td>383</td>
<td>335</td>
<td>382</td>
<td>336</td>
<td>382</td>
<td>336</td>
<td>112</td>
<td>383</td>
<td>335</td>
<td>382</td>
<td>336</td>
<td>382</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>112</td>
<td>550</td>
<td>337</td>
<td>547</td>
<td>339</td>
<td>547</td>
<td>339</td>
<td>112</td>
<td>550</td>
<td>337</td>
<td>547</td>
<td>339</td>
<td>547</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>112</td>
<td>320</td>
<td>916</td>
<td>319</td>
<td>920</td>
<td>319</td>
<td>920</td>
<td>112</td>
<td>320</td>
<td>916</td>
<td>319</td>
<td>920</td>
<td>319</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>112</td>
<td>511</td>
<td>237</td>
<td>516</td>
<td>234</td>
<td>516</td>
<td>234</td>
<td>112</td>
<td>515</td>
<td>235</td>
<td>515</td>
<td>235</td>
<td>514</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = 
  "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"
MALLOC_CONF = "retain:true"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 6348, 2.60GHz)

General Notes (Continued)

runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
UPI Link Enablement set to 1
UPI Power Management set to Enabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDDC Sparing set to Disabled
Patrol Scrub set to Disabled
Enhanced CPU performance set to Auto
Energy Efficient Turbo set to Enabled
Processor C6 Report set to Enabled
Processor C1E set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acfc64d
running on install Wed Jul 14 14:02:27 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
    model name : Intel(R) Xeon(R) Gold 6348 CPU @ 2.60GHz
    2 "physical id"s (chips)
    112 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 28
siblings : 56
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24

(Continued on next page)
CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

25 26 27
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
25 26 27

From lscpu from util-linux 2.33.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 112
On-line CPU(s) list: 0-111
Thread(s) per core: 2
Core(s) per socket: 28
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Gold 6348 CPU @ 2.60GHz
Stepping: 6
CPU MHz: 1064.562
CPU max MHz: 3500.0000
CPU min MHz: 800.0000
BogoMIPS: 5200.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 43008K
NUMA node0 CPU(s): 0-13, 56-69
NUMA node1 CPU(s): 14-27, 70-83
NUMA node2 CPU(s): 28-41, 84-97
NUMA node3 CPU(s): 42-55, 98-111

Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtrunc pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt ppest tsc_deadline_timer aes
xsave f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invpcid_single ssbd
mqa ibrs ibpb ibrs_endenhanced tpr_shadow vmni flexpriority ept vpid ept_ad
fsallbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqmm rdt_a avx512f
avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha_ni
avx512bw avx512v1 xsaves xsaveopt xsaves xsavec xgetbv1 xsaves cqmm_llc cqmm_occu
llc cqmm_mbmg_total

cqmm_local wbnoivd dtherm ida arat pln pts hwp hwp_act_window hwp_epp
hwp_pkg_req avx512v bmi umip pku ospke avx512_vbmi2 gfn vaes vpcm1ulqdq avx512_vnni
avx512_bitalg tme avx512_vpopcntdq la57 rdpid md_clear pconfig flush_l1d
arch_capabilities

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 6348, 2.60GHz)

SPEC CPU®2017 Integer Rate Result
Copyright 2017-2021 Standard Performance Evaluation Corporation

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Jul-2021
Tested by: Cisco Systems
Hardware Availability: Jun-2021
Software Availability: Mar-2021

SPECrate®2017_int_base = 424
SPECrate®2017_int_peak = 439

Platform Notes (Continued)

/pro cpuninfo cache data
  cache size : 43008 KB

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
  available: 4 nodes (0-3)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 56 57 58 59 60 61 62 63 64 65 66 67 68 69
  node 0 size: 515682 MB
  node 0 free: 515242 MB
  node 1 cpus: 14 15 16 17 18 19 20 21 22 23 24 25 26 27 70 71 72 73 74 75 76 77 78 79 80
  81 82 83
  node 1 size: 516055 MB
  node 1 free: 515680 MB
  node 2 cpus: 28 29 30 31 32 33 34 35 36 37 38 39 40 41 84 85 86 87 88 89 90 91 92 93 94
  95 96 97
  node 2 size: 516088 MB
  node 2 free: 515607 MB
  node 3 cpus: 42 43 44 45 46 47 48 49 50 51 52 53 54 55 98 99 100 101 102 103 104 105
  106 107 108 109 110 111
  node 3 size: 516085 MB
  node 3 free: 515798 MB
  node distances:
    node 0 1 2 3
    0: 10 11 20 20
    1: 11 10 20 20
    2: 20 20 10 11
    3: 20 20 11 10

From /proc/meminfo
  MemTotal: 2113445884 kB
  HugePages_Total: 0
  Hugepagesize: 2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15-SP2"
    VERSION_ID="15.2"
    PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15:sp2"

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 6348, 2.60GHz)

SPEC CPU®2017 Integer Rate Result
Copyright 2017-2021 Standard Performance Evaluation Corporation

SPECrate®2017_int_base = 424
SPECrate®2017_int_peak = 439

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jul-2021
Hardware Availability: Jun-2021
Software Availability: Mar-2021

Platform Notes (Continued)

uname -a:
    Linux install 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
    x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2018-3639 (Speculative Store Bypass): Mitigation: usercopy/swapgs barriers and __user pointer sanitization
CVE-2017-5753 (Spectre variant 1): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2017-5715 (Spectre variant 2):
CVE-2020-0543 (Special Register Buffer Data Sampling):
CVE-2019-11135 (TSX Asynchronous Abort):
run-level 3 Jul 14 13:44

SPEC is set to: /home/cpu2017
    Filesystem Type Size Used Avail Use% Mounted on
    /dev/sda2 btrfs 222G 37G 184G 17% /home

From /sys/devices/virtual/dmi/id
    Vendor: Cisco Systems Inc
    Product: UCSC-C240-M6S
    Serial: WZP24460JDZ

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
    32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200

BIOS:
    BIOS Vendor: Cisco Systems, Inc.
    BIOS Version: C240M6.4.2.1c.1.0701210708
    BIOS Date: 07/01/2021
    BIOS Revision: 5.22

(End of data from sysinfo program)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 6348, 2.60GHz)

<table>
<thead>
<tr>
<th>CPU2017 License: 9019</th>
<th>Test Date: Jul-2021</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor: Cisco Systems</td>
<td>Hardware Availability: Jun-2021</td>
</tr>
<tr>
<td>Tested by: Cisco Systems</td>
<td>Software Availability: Mar-2021</td>
</tr>
</tbody>
</table>

**Compiler Version Notes**

<table>
<thead>
<tr>
<th>C</th>
<th>500.perlbench_r(peak) 557.xz_r(peak)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000 Copyright (C) 1985-2020 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>C</th>
<th>502.gcc_r(peak)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version 2021.1 Build 20201113 Copyright (C) 1985-2020 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>C</th>
<th>500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak) 525.x264_r(base, peak) 557.xz_r(base)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113 Copyright (C) 1985-2020 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>C</th>
<th>500.perlbench_r(peak) 557.xz_r(peak)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000 Copyright (C) 1985-2020 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>C</th>
<th>502.gcc_r(peak)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version 2021.1 Build 20201113 Copyright (C) 1985-2020 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>C</th>
<th>500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak) 525.x264_r(base, peak) 557.xz_r(base)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113 Copyright (C) 1985-2020 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
</tbody>
</table>

(Spec CPU®2017 Integer Rate Result)

SPECRate®2017_int_base = 424
SPECRate®2017_int_peak = 439

(Continued on next page)
## SPEC CPU®2017 Integer Rate Result

**Cisco Systems**  
Cisco UCS C240 M6 (Intel Xeon Gold 6348, 2.60GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>SPECrate®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>= 424</td>
<td>= 439</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Test Date:** Jul-2021  
**Tested by:** Cisco Systems  
**Hardware Availability:** Jun-2021  
**Software Availability:** Mar-2021

---

**Compiler Version Notes (Continued)**

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

---

<table>
<thead>
<tr>
<th>C</th>
<th>500.perlbench_r (peak) 557.xz_r (peak)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000</td>
<td></td>
</tr>
<tr>
<td>Copyright (C) 1985-2020 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
</tbody>
</table>

---

<table>
<thead>
<tr>
<th>C</th>
<th>502.gcc_r (peak)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version 2021.1 Build 20201113</td>
<td></td>
</tr>
<tr>
<td>Copyright (C) 1985-2020 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
</tbody>
</table>

---

<table>
<thead>
<tr>
<th>C</th>
<th>500.perlbench_r (base) 502.gcc_r (base) 505.mcf_r (base, peak)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113</td>
<td></td>
</tr>
<tr>
<td>Copyright (C) 1985-2020 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
</tbody>
</table>

---

<table>
<thead>
<tr>
<th>C++</th>
<th>520.omnetpp_r (base, peak) 523.xalancbmk_r (base, peak)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113</td>
<td></td>
</tr>
<tr>
<td>Copyright (C) 1985-2020 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
</tbody>
</table>

---

<table>
<thead>
<tr>
<th>Fortran</th>
<th>548.exchange2_r (base, peak)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000</td>
<td></td>
</tr>
<tr>
<td>Copyright (C) 1985-2020 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
</tbody>
</table>
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 6348, 2.60GHz)

SPEC®2017 Integer Rate Result
Copyright 2017-2021 Standard Performance Evaluation Corporation

SPECrate®2017_int_base = 424
SPECrate®2017_int_peak = 439

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Jul-2021
Hardware Availability: Jun-2021
Software Availability: Mar-2021

Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Base Portability Flags
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags
C benchmarks:
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

C++ benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

Fortran benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-auto -mbranches-within-32B-boundaries

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 6348, 2.60GHz)

SPECrated®2017_int_base = 424
SPECrated®2017_int_peak = 439

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Jul-2021
Hardware Availability: Jun-2021
Tested by: Cisco Systems
Software Availability: Mar-2021

Base Optimization Flags (Continued)

Fortran benchmarks (continued):
-1/\text{l}/\text{opt}/\text{intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-1qkmalloc

Peak Compiler Invocation

C benchmarks (except as noted below):
icx
500.perlbench_r: ic
557.xz_r: ic

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Peak Portability Flags

500.perlbench_r: -DSPEC\_LP64 -DSPEC\_LINUX\_X64
502.gcc_r: -D\_FILE\_OFFSET\_BITS=64
505.mcf_r: -DSPEC\_LP64
520.omnetpp_r: -DSPEC\_LP64
523.xalancbmk_r: -DSPEC\_LP64 -DSPEC\_LINUX
525.x264_r: -DSPEC\_LP64
531.deepsjeng_r: -DSPEC\_LP64
541.leela_r: -DSPEC\_LP64
548.exchange2_r: -DSPEC\_LP64
557.xz_r: -DSPEC\_LP64

Peak Optimization Flags

C benchmarks:
500.perlbench_r: -Wl, -z, muldefs -prof-gen(pass 1) -prof-use(pass 2)
-xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-strict-overflow
-mbranches-within-32B-boundaries

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 6348, 2.60GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>424</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_int_peak</td>
<td>439</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Test Date:</td>
<td>Jul-2021</td>
</tr>
<tr>
<td>Hardware Availability:</td>
<td>Jun-2021</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>Mar-2021</td>
</tr>
</tbody>
</table>

**Peak Optimization Flags (Continued)**

500.perlbench_r (continued):
- `L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin`
- `-lqkmalloc`

502.gcc_r: `-m32`
- `L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/ia32_lin`
- `-std=gnu89 -Wl,-z,muldefs -fprofile-generate(pass 1)`
- `-fprofile-use=default.profdata(pass 2) -xCORE-AVX512 -flto`
- `-O3 -ffast-math -qopt-mem-layout-trans=4`
- `-mbranches-within-32B-boundaries`
- `-L/usr/local/jemalloc32-5.0.1/lib -ljemalloc`

505.mcf_r: basepeak = yes

525.x264_r: `-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -flto`
- `-O3 -ffast-math -qopt-mem-layout-trans=4 -fno-alias`
- `-mbranches-within-32B-boundaries`
- `-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin`
- `-lqkmalloc`

557.xz_r: `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
- `-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries`
- `-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin`
- `-lqkmalloc`

C++ benchmarks:

520.omnetpp_r: basepeak = yes

523.xalancbmk_r: basepeak = yes

531.deepsjeng_r: basepeak = yes

541.leela_r: basepeak = yes

Fortran benchmarks:

548.exchange2_r: basepeak = yes

The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links:

http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.0-ICX-revF.xml
## SPEC CPU®2017 Integer Rate Result

**Cisco Systems**

Cisco UCS C240 M6 (Intel Xeon Gold 6348, 2.60GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>424</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_int_peak</td>
<td>439</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Test Date:</th>
<th>Jul-2021</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hardware Availability:</td>
<td>Jun-2021</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>Mar-2021</td>
</tr>
</tbody>
</table>

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.8 on 2021-07-14 14:02:27-0400.
Report generated on 2021-08-04 18:21:33 by CPU2017 PDF formatter v6442.
Originally published on 2021-08-04.