Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 6342, 2.80GHz)

**SPECrate®2017_int_base = 382**
**SPECrate®2017_int_peak = 396**

<table>
<thead>
<tr>
<th>Copies</th>
<th>CPU2017 License: 9019</th>
<th>Test Date: Jul-2021</th>
</tr>
</thead>
<tbody>
<tr>
<td>96</td>
<td>Test Sponsor: Cisco Systems</td>
<td>Hardware Availability: Jun-2021</td>
</tr>
<tr>
<td></td>
<td>Tested by: Cisco Systems</td>
<td>Software Availability: Mar-2021</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base (382)</th>
<th>SPECrate®2017_int_peak (396)</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r 96</td>
<td>500.perlbench_r 96</td>
</tr>
<tr>
<td>502.gcc_r 96</td>
<td>502.gcc_r 96</td>
</tr>
<tr>
<td>505.mcf_r 96</td>
<td>505.mcf_r 96</td>
</tr>
<tr>
<td>520.omnetpp_r 96</td>
<td>520.omnetpp_r 96</td>
</tr>
<tr>
<td>523.xalancbmk_r 96</td>
<td>523.xalancbmk_r 96</td>
</tr>
<tr>
<td>525.x264_r 96</td>
<td>525.x264_r 96</td>
</tr>
<tr>
<td>531.deepsjeng_r 96</td>
<td>531.deepsjeng_r 96</td>
</tr>
<tr>
<td>541.leela_r 96</td>
<td>541.leela_r 96</td>
</tr>
<tr>
<td>548.exchange2_r 96</td>
<td>548.exchange2_r 96</td>
</tr>
<tr>
<td>557.xz_r 96</td>
<td>557.xz_r 96</td>
</tr>
</tbody>
</table>

### Hardware
- **CPU Name:** Intel Xeon Gold 6342
- **Max MHz:** 3500
- **Nominal:** 2800
- **Enabled:** 48 cores, 2 chips, 2 threads/core
- **Orderable:** 1.2 Chips
- **Cache L1:** 32 KB I + 48 KB D on chip per core
- **L2:** 1.25 MB I+D on chip per core
- **L3:** 36 MB I+D on chip per chip
- **Other:** None
- **Memory:** 2 TB (32 x 64 GB 2Rx4 PC4-3200AA-R)
- **Storage:** 1 x 300 GB 15K SAS HDD
- **Other:** None

### Software
- **OS:** SUSE Linux Enterprise Server 15 SP2
- **Compiler:** C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux; Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux; C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux
- **Parallel:** No
- **Firmware:** Version 4.2.1c released Jul-2021
- **File System:** btrfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 32/64-bit
- **Other:** jemalloc memory allocator V5.0.1
- **Power Management:** BIOS and OS set to prefer performance at the cost of additional power usage
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 6342, 2.80GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>96</td>
<td>578</td>
<td>264</td>
<td>578</td>
<td>264</td>
<td>579</td>
<td>264</td>
<td>96</td>
<td>495</td>
<td>309</td>
<td>494</td>
<td>309</td>
<td>494</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>96</td>
<td>451</td>
<td>301</td>
<td>449</td>
<td>303</td>
<td>452</td>
<td>301</td>
<td>96</td>
<td>379</td>
<td>359</td>
<td>381</td>
<td>357</td>
<td>381</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>96</td>
<td>239</td>
<td>649</td>
<td>240</td>
<td>646</td>
<td>239</td>
<td>649</td>
<td>96</td>
<td>239</td>
<td>649</td>
<td>240</td>
<td>646</td>
<td>239</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>96</td>
<td>563</td>
<td>224</td>
<td>563</td>
<td>224</td>
<td>565</td>
<td>223</td>
<td>96</td>
<td>563</td>
<td>224</td>
<td>563</td>
<td>224</td>
<td>563</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>96</td>
<td>207</td>
<td>490</td>
<td>208</td>
<td>487</td>
<td>208</td>
<td>488</td>
<td>96</td>
<td>207</td>
<td>490</td>
<td>208</td>
<td>487</td>
<td>208</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>96</td>
<td>208</td>
<td>810</td>
<td>209</td>
<td>805</td>
<td>209</td>
<td>806</td>
<td>96</td>
<td>199</td>
<td>845</td>
<td>199</td>
<td>845</td>
<td>199</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>96</td>
<td>372</td>
<td>296</td>
<td>372</td>
<td>295</td>
<td>372</td>
<td>296</td>
<td>96</td>
<td>372</td>
<td>296</td>
<td>372</td>
<td>295</td>
<td>372</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>96</td>
<td>547</td>
<td>290</td>
<td>548</td>
<td>290</td>
<td>549</td>
<td>290</td>
<td>96</td>
<td>547</td>
<td>290</td>
<td>548</td>
<td>290</td>
<td>549</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>96</td>
<td>314</td>
<td>802</td>
<td>313</td>
<td>802</td>
<td>313</td>
<td>802</td>
<td>96</td>
<td>314</td>
<td>802</td>
<td>313</td>
<td>802</td>
<td>313</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>96</td>
<td>493</td>
<td>210</td>
<td>493</td>
<td>210</td>
<td>493</td>
<td>210</td>
<td>96</td>
<td>502</td>
<td>207</td>
<td>503</td>
<td>206</td>
<td>501</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = 
  "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"
MALLOC_CONF = "retain:true"

General Notes
Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM
memory using opensUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 6342, 2.80GHz)

SPECrater®2017_int_base = 382
SPECrater®2017_int_peak = 396

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jul-2021
Hardware Availability: Jun-2021
Software Availability: Mar-2021

General Notes (Continued)

runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
UPI Link Enablement set to 1
UPI Power Management set to Enabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDC Sparing set to Disabled
Patrol Scrub set to Disabled
Enhanced CPU performance set to Auto
Energy Efficient Turbo set to Enabled
Processor C6 Report set to Enabled
Processor C1E set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d
running on install Fri Jul 9 17:41:46 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
  model name : Intel(R) Xeon(R) Gold 6342 CPU @ 2.80GHz
    2 "physical id"s (chips)
    96 "processors"
  cores, siblings (Caution: counting these is hw and system dependent. The following
  excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
    cpu cores : 24
    siblings : 48
    physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 6342, 2.80GHz)

SPECrate®2017_int_base = 382
SPECrate®2017_int_peak = 396

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Jul-2021
Hardware Availability: Jun-2021
Tested by: Cisco Systems
Software Availability: Mar-2021

Platform Notes (Continued)

physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23

From lscpu from util-linux 2.33.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 96
On-line CPU(s) list: 0-95
Thread(s) per core: 2
Core(s) per socket: 24
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Gold 6342 CPU @ 2.80GHz
Stepping: 6
CPU MHz: 800.050
CPU max MHz: 3500.0000
CPU min MHz: 800.0000
BogoMIPS: 5600.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 36864K
NUMA node0 CPU(s): 0-11,48-59
NUMA node1 CPU(s): 12-23,60-71
NUMA node2 CPU(s): 24-35,72-83
NUMA node3 CPU(s): 36-47,84-95
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdflush cgroup
lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpref pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtpr pdcm pclid dca sse4_1 sse4_2 x2apic movbe poprd popcnt tsdiag dead_line_timer aes
xsave f16c rdrand lahf_l1met abm 3dnowprefetch cpuid_fault ept cat_13 invpcl_single ssbd
mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi flexpriority ept vpid ept_ad
fsgsbase tsc_adjust bni hle avx2 smep bmi2 erms invpcid rtm cqm rdt_a avx512f
avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha ni
avx512bw avx512vl xsaveopt xsave cxtbx xsavec cqm_llc cqm_occup_llc cqm_mbm_total
cqm_mbm_local wbinvd dtherm ida arat pln pts hwp hwp_act_window hwp_epp
hwp_pkg_req avx512vbmi umip pku ospke ospk avx512v bmi2 gfn faes vpclmulqdq avx512_vnni
avx512_bitalg tme avx512_vpopcntdq 1a57 rdpid md_clear pconfig flush_l1d
arch_capabilities

/proc/cpuinfo cache data

(Continued on next page)
Cisco Systems

Cisco UCS C240 M6 (Intel Xeon Gold 6342, 2.80GHz)

SPECrate®2017_int_base = 382
SPECrate®2017_int_peak = 396

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

cache size : 36864 KB

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 48 49 50 51 52 53 54 55 56 57 58 59
node 0 size: 515682 MB
node 0 free: 515322 MB
node 1 cpus: 12 13 14 15 16 17 18 19 20 21 22 23 60 61 62 63 64 65 66 67 68 69 70 71
node 1 size: 516056 MB
node 1 free: 515634 MB
node 2 cpus: 24 25 26 27 28 29 30 31 32 33 34 35 72 73 74 75 76 77 78 79 80 81 82 83
node 2 size: 516089 MB
node 2 free: 515823 MB
node 3 cpus: 36 37 38 39 40 41 42 43 44 45 46 47 84 85 86 87 88 89 90 91 92 93 94 95
node 3 size: 516086 MB
node 3 free: 515308 MB
node distances:
node 0 1 2 3
0: 10 11 20 20
1: 11 10 20 20
2: 20 20 10 11
3: 20 20 11 10

From /proc/meminfo
MemTotal: 2113449256 kB
HugePages_Total: 0
Hugepagesize: 2048 kB
/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15-SP2"
VERSION_ID="15.2"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
Linux install 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
x86_64 x86_64 GNU/Linux

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 6342, 2.80GHz)  

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>SPECrate®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>382</td>
<td>396</td>
</tr>
</tbody>
</table>

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems  

Test Date: Jul-2021  
Hardware Availability: Jun-2021  
Software Availability: Mar-2021

Platform Notes (Continued)

Kernel self-reported vulnerability status:

- CVE-2018-12207 (iTLB Multihit): Not affected
- CVE-2018-3620 (L1 Terminal Fault): Not affected
- Microarchitectural Data Sampling: Not affected
- CVE-2017-5754 (Meltdown): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
- CVE-2018-3639 (Speculative Store Bypass): Mitigation: usercopy/swapgs barriers and __user pointer sanitization
- CVE-2017-5753 (Spectre variant 1): Not affected
- CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
- CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
- CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Jul 9 17:23

SPEC is set to: /home/cpu2017

<table>
<thead>
<tr>
<th>Filesystem</th>
<th>Type</th>
<th>Size</th>
<th>Used</th>
<th>Avail</th>
<th>Use%</th>
<th>Mounted on</th>
</tr>
</thead>
<tbody>
<tr>
<td>/dev/sdc2</td>
<td>btrfs</td>
<td>277G</td>
<td>26G</td>
<td>248G</td>
<td>10%</td>
<td>/home</td>
</tr>
</tbody>
</table>

From /sys/devices/virtual/dmi/id

Vendor: Cisco Systems Inc  
Product: UCSC-C240-M6SX  
Serial: WZP244208SJ

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:

- 32x 0xCE00 M393A8G40AB2-CWE 64 GB 2 rank 3200

BIOS:

- BIOS Vendor: Cisco Systems, Inc.
- BIOS Version: C240M6.4.2.1c.1.0701210708
- BIOS Date: 07/01/2021
- BIOS Revision: 5.22

(End of data from sysinfo program)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 6342, 2.80GHz)

SPECrater®2017_int_base = 382
SPECrater®2017_int_peak = 396

CPU2017 License: 9019
Test Date: Jul-2021
Test Sponsor: Cisco Systems
Hardware Availability: Jun-2021
Tested by: Cisco Systems
Software Availability: Mar-2021

Compiler Version Notes

==============================================================================
| C | 500.perlbench_r(peak) 557.xz_r(peak)
| Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
  64, Version 2021.1 Build 20201112_000000
| Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================

| C | 502.gcc_r(peak)
| Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version
  2021.1 Build 20201113
| Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================

| C | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
  | 525.x264_r(base, peak) 557.xz_r(base)
| Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
| Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================

| C | 500.perlbench_r(peak) 557.xz_r(peak)
| Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
  64, Version 2021.1 Build 20201112_000000
| Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================

| C | 502.gcc_r(peak)
| Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version
  2021.1 Build 20201113
| Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================

| C | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
  | 525.x264_r(base, peak) 557.xz_r(base)
| Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 6342, 2.80GHz)

**SPEC CPU®2017 Integer Rate Result**

<table>
<thead>
<tr>
<th>Test Sponsor</th>
<th>CPU2017 License</th>
<th>Tested by</th>
<th>Hardware Availability</th>
<th>Software Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cisco Systems</td>
<td>9019</td>
<td>Cisco Systems</td>
<td>Jun-2021</td>
<td>Mar-2021</td>
</tr>
</tbody>
</table>

**SPECrate®2017_int_base = 382**
**SPECrate®2017_int_peak = 396**

<table>
<thead>
<tr>
<th>Compiler Version</th>
<th>SPECrate®2017_int_base</th>
<th>SPECrate®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td>500.perlbench_r(peak)</td>
<td>557.xz_r(peak)</td>
</tr>
<tr>
<td>Intel(R) C</td>
<td>502.gcc_r(peak)</td>
<td></td>
</tr>
<tr>
<td>Intel(R) oneAPI</td>
<td>500.perlbench_r(base)</td>
<td>502.gcc_r(base)</td>
</tr>
<tr>
<td>Intel(R) oneAPI</td>
<td>505.mcf_r(base, peak)</td>
<td>525.x264_r(base, peak)</td>
</tr>
<tr>
<td>Intel(R) oneAPI</td>
<td>523.xalancbmk_r(base, peak)</td>
<td>531.deepsjeng_r(base, peak)</td>
</tr>
<tr>
<td>Intel(R) oneAPI</td>
<td>541.leela_r(base, peak)</td>
<td></td>
</tr>
<tr>
<td>Fortran</td>
<td>548.exchange2_r(base, peak)</td>
<td></td>
</tr>
</tbody>
</table>

---

**Compiler Version Notes (Continued)**

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

---

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

---

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

---

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

---

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

---

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
## Cisco Systems

Cisco UCS C240 M6 (Intel Xeon Gold 6342, 2.80GHz)  

<table>
<thead>
<tr>
<th>CPU2017 License</th>
<th>Test Date</th>
<th>Test Sponsor</th>
<th>Hardware Availability</th>
<th>Tested by</th>
<th>Software Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td>9019</td>
<td>Jul-2021</td>
<td>Cisco Systems</td>
<td>Jun-2021</td>
<td>Cisco Systems</td>
<td>Mar-2021</td>
</tr>
</tbody>
</table>

### SPECrate®2017_int_base = 382  
### SPECrate®2017_int_peak = 396

### Base Compiler Invocation

- **C benchmarks:**
  - icx

- **C++ benchmarks:**
  - icpx

- **Fortran benchmarks:**
  - ifort

### Base Portability Flags

```
500.perlbuch_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalanchmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64
```

### Base Optimization Flags

- **C benchmarks:**
  ```
  -w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math
  -flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
  -mbranches-within-32B-boundaries
  -L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
  -lqkmalloc
  ```

- **C++ benchmarks:**
  ```
  -w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math -flto
  -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
  -mbranches-within-32B-boundaries
  -L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
  -lqkmalloc
  ```

- **Fortran benchmarks:**
  ```
  -w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
  -qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
  -auto -mbranches-within-32B-boundaries
  ```

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 6342, 2.80GHz)

SPECrater®2017_int_base = 382
SPECrater®2017_int_peak = 396

Base Optimization Flags (Continued)
Fortran benchmarks (continued):
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

Peak Compiler Invocation
C benchmarks (except as noted below):
icx
500.perlbench_r: icc
557.xz_r: icc

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Peak Portability Flags
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSEQUENCE
520.omnetpp_r: -DSEQUENCE
523.xalancbmk_r: -DSEQUENCE
525.x264_r: -DSEQUENCE
531.deepsjeng_r: -DSEQUENCE
541.leela_r: -DSEQUENCE
548.exchange2_r: -DSEQUENCE
557.xz_r: -DSEQUENCE

Peak Optimization Flags
C benchmarks:
500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)
-xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-strict-overflow
-mbranches-within-32B-boundaries

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 6342, 2.80GHz)

Peak Optimization Flags (Continued)

500.perlbench_r (continued):
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

502.gcc_r: -m32
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/ia32_lin
-std=gnu89 -Wl,-z,muldefs -fprofile-generate(pass1)
-ffast-math -O3 -fast -g -fno-alias -mbranches-within-32B-boundaries
-L/usr/local/jemalloc32-5.0.1/lib -ljemalloc

505.mcf_r: basepeak = yes

525.x264_r: -w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -flto
-O3 -ffast-math -g -fno-alias -mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

C++ benchmarks:
520.omnetpp_r: basepeak = yes
523.xalancbmk_r: basepeak = yes
531.deepsjeng_r: basepeak = yes
541.leela_r: basepeak = yes

Fortran benchmarks:
548.exchange2_r: basepeak = yes

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.0-ICX-revF.xml
## SPEC CPU®2017 Integer Rate Result

**Vendor:** Cisco Systems  
**System:** Cisco UCS C240 M6 (Intel Xeon Gold 6342, 2.80GHz)  
**Tested with:** SPEC CPU®2017 v1.1.8 on 2021-07-09 20:41:45-0400.  
**Report generated on:** 2021-08-04 18:21:33 by CPU2017 PDF formatter v6442.  
**Originally published on:** 2021-08-04.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_int_base</td>
<td>382</td>
</tr>
<tr>
<td>SPECrate®2017_int_peak</td>
<td>396</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Jul-2021  
**Hardware Availability:** Jun-2021  
**Software Availability:** Mar-2021

---

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

---

Report generated on 2021-08-04 18:21:33 by CPU2017 PDF formatter v6442.