Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 6354, 3.00GHz)

SPECrate\textsuperscript{®}2017\textsubscript{int\_peak} = 321
SPECrate\textsuperscript{®}2017\textsubscript{int\_base} = 310


cpu2017 license: 9019
test sponsor: Cisco Systems
tested by: Cisco Systems
test date: Jul-2021
hardware availability: Jun-2021
software availability: Mar-2021

<table>
<thead>
<tr>
<th>Program</th>
<th>Copies</th>
<th>SPECrate\textsuperscript{®}2017\textsubscript{int_base} (310)</th>
<th>SPECrate\textsuperscript{®}2017\textsubscript{int_peak} (321)</th>
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<tr>
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<tr>
<td>548.exchange2_r</td>
<td>72</td>
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<tr>
<td>557.xz_r</td>
<td>72</td>
<td>167</td>
<td>644</td>
</tr>
</tbody>
</table>

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**Hardware**

CPU Name: Intel Xeon Gold 6354
Max MHz: 3600
Nominal: 3000
Enabled: 36 cores, 2 chips, 2 threads/core
Orderable: 1.2 Chips
Cache L1: 32 KB I + 48 KB D on chip per core
L2: 1.25 MB I+D on chip per core
L3: 39 MB I+D on chip per chip
Other: None
Memory: 1 TB (32 x 32 GB 2Rx4 PC4-3200AA-R)
Storage: 1 x 240 GB SATA SSD
Other: None

**Software**

OS: SUSE Linux Enterprise Server 15 SP2
5.3.18-22-default
Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++
Compiler Build 20201113 for Linux;
Fortran: Version 2021.1 of Intel Fortran Compiler
Classic Build 20201112 for Linux;
C/C++: Version 2021.1 of Intel C/C++ Compiler
Classic Build 20201112 for Linux
Parallel: No
Firmware: Version 4.2.1c released Jul-2021
File System: btrfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 32/64-bit
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS and OS set to prefer performance at the cost of additional power usage
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 6354, 3.00GHz)

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
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<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
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</tbody>
</table>

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH =
"/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"
MALLOC_CONF = "retain:true"

General Notes
Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM
memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 6354, 3.00GHz)

SPEC CPU®2017 Integer Rate Result

SPECrate®2017_int_base = 310
SPECrate®2017_int_peak = 321

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

General Notes (Continued)

runcpu command invoked through numactl i.e.: numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
UPI Link Enablement set to 1
UPI Power Management set to Enabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDDC Sparing set to Disabled
Patrol Scrub set to Disabled
Enhanced CPU performance set to Auto
Energy Efficient Turbo set to Enabled
Processor C6 Report set to Enabled
Processor C1E set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16aca64d
running on install Sun Jul  4 19:50:13 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6354 CPU @ 3.00GHz
  2  "physical id"s (chips)
  72 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 18
siblings : 36
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17

(Continued on next page)
Platform Notes (Continued)

From lscpu from util-linux 2.33.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 72
On-line CPU(s) list: 0-71
Thread(s) per core: 2
Core(s) per socket: 18
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Gold 6354 CPU @ 3.00GHz
Stepping: 6
CPU MHz: 799.980
CPU max MHz: 3600.0000
CPU min MHz: 800.0000
BogoMIPS: 6000.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 39936K
NUMA node0 CPU(s): 0-8,36-44
NUMA node1 CPU(s): 9-17,45-53
NUMA node2 CPU(s): 18-26,54-62
NUMA node3 CPU(s): 27-35,63-71
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aerpmpref pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtrp pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invpcid_single ssbd
mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vmmi flexpriority ept vpid ept_ad
fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm rdt_a avx512f
avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha ni
avx512bw avx512vli xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbb_total
cqm_mbb_local wbnoinvd dtherm ida arat pln pts hwp hwp_act_window hwp_epp
hwp_pkg_req avx512vbm1 umip pkd ospk avx512vbm12 gfn i vaes vcplmulqdq avx512_vnni
avx512_bitalg tme avx512_vpopcntdq la57 rdpid md_clear pconfig flush_l1d
arch_capabilities

/proc/cpuinfo cache data

(Continued on next page)
Platform Notes (Continued)

```plaintext
From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 4 nodes (0-3)
 node 0 cpus: 0 1 2 3 4 5 6 7 8 36 37 38 39 40 41 42 43 44
 node 0 size: 257636 MB
 node 0 free: 257332 MB
 node 1 cpus: 9 10 11 12 13 14 15 16 17 45 46 47 48 49 50 51 52 53
 node 1 size: 258043 MB
 node 1 free: 257621 MB
 node 2 cpus: 18 19 20 21 22 23 24 25 26 54 55 56 57 58 59 60 61 62
 node 2 size: 258009 MB
 node 2 free: 257547 MB
 node 3 cpus: 27 28 29 30 31 32 33 34 35 63 64 65 66 67 68 69 70 71
 node 3 size: 258039 MB
 node 3 free: 257706 MB
 node distances:
 node   0   1   2   3
 0:  10  11  20  20
 1:  11  10  20  20
 2:  20  20  10  11
 3:  20  20  11  10

From /proc/meminfo
MemTotal:       1056491476 kB
 HugePages_Total:       0
 Hugepagesize:       2048 kB
/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release*/etc/*version*
os-release:
 NAME="SLES"
 VERSION="15-SP2"
 VERSION_ID="15.2"
 PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
 ID="sles"
 ID_LIKE="suse"
 ANSI_COLOR="0;32"
 CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
 Linux install 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
 x86_64 x86_64 GNU/Linux
```

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 6354, 3.00GHz)

| SPECrate®2017_int_base = 310 |
| SPECrate®2017_int_peak = 321 |

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems

| Test Date: | Jul-2021 |
| Hardware Availability: | Jun-2021 |
| Software Availability: | Mar-2021 |

**Platform Notes (Continued)**

Kernel self-reported vulnerability status:

<table>
<thead>
<tr>
<th>Vulnerability</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>CVE-2018-12207 (iTLB Multihit):</td>
<td>Not affected</td>
</tr>
<tr>
<td>CVE-2018-3620 (L1 Terminal Fault):</td>
<td>Not affected</td>
</tr>
<tr>
<td>Microarchitectural Data Sampling:</td>
<td>Not affected</td>
</tr>
<tr>
<td>CVE-2017-5754 (Meltdown):</td>
<td>Not affected</td>
</tr>
<tr>
<td>CVE-2018-3639 (Speculative Store Bypass):</td>
<td>Mitigation: Speculative Store Bypass disabled via prctl and seccomp</td>
</tr>
<tr>
<td>CVE-2017-5753 (Spectre variant 1):</td>
<td>Mitigation: usercopy/swaps barriers and __user pointer sanitation</td>
</tr>
<tr>
<td>CVE-2017-5715 (Spectre variant 2):</td>
<td>Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling</td>
</tr>
<tr>
<td>CVE-2020-0543 (Special Register Buffer Data Sampling):</td>
<td>Not affected</td>
</tr>
<tr>
<td>CVE-2019-11135 (TSX Asynchronous Abort):</td>
<td>Not affected</td>
</tr>
</tbody>
</table>

run-level 3 Jul 4 19:47

SPEC is set to: /home/cpu2017

<table>
<thead>
<tr>
<th>Filesystem</th>
<th>Type</th>
<th>Size</th>
<th>Used</th>
<th>Avail</th>
<th>Use%</th>
<th>Mounted on</th>
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</thead>
<tbody>
<tr>
<td>/dev/sda2</td>
<td>btrfs</td>
<td>222G</td>
<td>37G</td>
<td>184G</td>
<td>17%</td>
<td>/home</td>
</tr>
</tbody>
</table>

From /sys/devices/virtual/dmi/id

<table>
<thead>
<tr>
<th>Field</th>
<th>Value</th>
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</thead>
<tbody>
<tr>
<td>Vendor</td>
<td>Cisco Systems Inc</td>
</tr>
<tr>
<td>Product</td>
<td>UCSC-C240-M6S</td>
</tr>
<tr>
<td>Serial</td>
<td>WZP24460JDZ</td>
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</tbody>
</table>

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory: 32x 0xCE00 M393A4K40DB3-CWE 32 GB 2 rank 3200

BIOS:

<table>
<thead>
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<th>Field</th>
<th>Value</th>
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<td>BIOS Version</td>
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<tr>
<td>BIOS Date</td>
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<td>BIOS Revision</td>
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(End of data from sysinfo program)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 6354, 3.00GHz)

SPECrater®2017_int_base = 310
SPECrater®2017_int_peak = 321

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Tested by: Cisco Systems
Hardware Availability: Jun-2021
Software Availability: Mar-2021

Compiler Version Notes

==============================================================================
C       | 500.perlbench_r(peak) 557.xz_r(peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
  64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
-----------------------------------------------------------------------------

C       | 502.gcc_r(peak)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version
  2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
-----------------------------------------------------------------------------

C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
         | 525.x264_r(base, peak) 557.xz_r(base)
------------------------------------------------------------------------------
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(Continued on next page)
**Cisco Systems**

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**SPECrate®2017_int_base = 310**

**SPECrate®2017_int_peak = 321**

**Compiler Version Notes (Continued)**

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<tr>
<th>Language</th>
<th>Test</th>
<th>Compiler</th>
<th>Version</th>
<th>Availability</th>
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<td>C</td>
<td>500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak) 525.x264_r(base, peak) 557.xz_r(base)</td>
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<td>Copyright (C) 1985-2020 Intel Corporation. All rights reserved.</td>
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Tested by: Cisco Systems  

Test Date: Jul-2021  
Hardware Availability: Jun-2021  
Software Availability: Mar-2021

### Base Compiler Invocation

C benchmarks:  
icc

C++ benchmarks:  
icpx

Fortran benchmarks:  
ifort

### Base Portability Flags

- 500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
- 502.gcc_r: -DSPEC_LP64
- 505.mcf_r: -DSPEC_LP64
- 520.omnetpp_r: -DSPEC_LP64
- 523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
- 525.x264_r: -DSPEC_LP64
- 531.deepsjeng_r: -DSPEC_LP64
- 541.leela_r: -DSPEC_LP64
- 548.exchange2_r: -DSPEC_LP64
- 557.xz_r: -DSPEC_LP64

### Base Optimization Flags

**C benchmarks:**  
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math  
-ftlo -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4  
-mbranches-within-32B-boundaries  
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin  
-lqkmalloc

**C++ benchmarks:**  
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math -f1to  
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4  
-mbranches-within-32B-boundaries  
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin  
-lqkmalloc

**Fortran benchmarks:**  
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div  
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte  
-auto -mbranches-within-32B-boundaries

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SPEC CPU®2017 Integer Rate Result

Cisco Systems

Cisco UCS C240 M6 (Intel Xeon Gold 6354, 3.00GHz)

| SPECrate®2017_int_base = 310 |
| SPECrate®2017_int_peak = 321 |

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jul-2021
Hardware Availability: Jun-2021
Software Availability: Mar-2021

Base Optimization Flags (Continued)

Fortran benchmarks (continued):
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

Peak Compiler Invocation

C benchmarks (except as noted below):
icx

500.perlbench_r: icc

557.xz_r: icc

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:

500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)
-xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-strict-overflow
-mbranches-within-32B-boundaries

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Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 6354, 3.00GHz)

SPEC CPU®2017 Integer Rate Result
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Peak Optimization Flags (Continued)

500.perlbench_r (continued):
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

502.gcc_r: -m32
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/ia32_lin
-std=gnu89 -Wl,-z,muldefs -fprofile=generate(pass1)
-fprofile-use=default.profdata(pass 2) -xCORE-AVX512 -flto
-O2 -Wl,-z,muldefs -fprofile-use=default.profdata(pass 3) -flto

505.mcf_r: basepeak = yes

525.x264_r: -w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -flto
-O3 -ffast-math -gopt-mem-layout-trans=4 -fno-alias
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

557.xz_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-gopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

C++ benchmarks:

520.omnetpp_r: basepeak = yes

523.xalancbmk_r: basepeak = yes

531.deepsjeng_r: basepeak = yes

541.leela_r: basepeak = yes

Fortran benchmarks:

548.exchange2_r: basepeak = yes

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.0-ICX-revF.xml
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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.