Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 6338, 2.00GHz)

<table>
<thead>
<tr>
<th>Software</th>
<th>Hardware</th>
</tr>
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<tbody>
<tr>
<td>OS: SUSE Linux Enterprise Server 15 SP2 5.3.18-22-default</td>
<td>CPU Name: Intel Xeon Gold 6338</td>
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<tr>
<td>Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux; Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux;</td>
<td>Max MHz: 3200</td>
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<tr>
<td>Firmware: Version 4.2.1c released Jul-2021</td>
<td>Nominal: 2000</td>
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<tr>
<td>File System: btrfs</td>
<td>Enabled: 64 cores, 2 chips, 2 threads/core</td>
</tr>
<tr>
<td>System State: Run level 3 (multi-user)</td>
<td>Orderable: 1,2 Chips</td>
</tr>
<tr>
<td>Base Pointers: 64-bit</td>
<td>Cache L1: 32 KB I + 48 KB D on chip per core</td>
</tr>
<tr>
<td>Peak Pointers: Not Applicable</td>
<td>L2: 1.25 MB I+D on chip per core</td>
</tr>
<tr>
<td>Other: jemalloc memory allocator V5.0.1</td>
<td>L3: 48 MB I+D on chip per chip</td>
</tr>
<tr>
<td>Power Management: BIOS and OS set to prefer performance at the cost of additional power usage</td>
<td>Memory: 1 TB (32 x 32 GB 2Rx4 PC4-3200AA-R)</td>
</tr>
<tr>
<td></td>
<td>Storage: 1 x 300 GB 15K SAS HDD</td>
</tr>
<tr>
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<td>Other: None</td>
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SPECratenet®2017_fp_base = 388
SPECratenet®2017_fp_peak = Not Run

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<tr>
<td>507.cactuBSSN_r</td>
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<tr>
<td>508.namd_r</td>
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<tr>
<td>510.parest_r</td>
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<tr>
<td>511.povray_r</td>
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<tr>
<td>519.lbm_r</td>
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<tr>
<td>521.wrf_r</td>
</tr>
<tr>
<td>526.blender_r</td>
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<td>527.cam4_r</td>
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<td>549.fotonik3d_r</td>
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<tr>
<td>554.roms_r</td>
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Test Date: Jul-2021
Hardware Availability: Jun-2021
Software Availability: Mar-2021

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

- 503.bwaves_r: 737
- 507.cactuBSSN_r: 538
- 508.namd_r: 299
- 510.parest_r: 203
- 511.povray_r: 448
- 519.lbm_r: 268
- 521.wrf_r: 346
- 526.blender_r: 420
- 527.cam4_r: 412
- 538.imagick_r: 1050
- 544.nab_r: 679
- 549.fotonik3d_r: 233
- 554.roms_r: 157

Software

- OS: SUSE Linux Enterprise Server 15 SP2 5.3.18-22-default
- Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux; Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux;
- Firmware: Version 4.2.1c released Jul-2021
- File System: btrfs
- System State: Run level 3 (multi-user)
- Base Pointers: 64-bit
- Peak Pointers: Not Applicable
- Other: jemalloc memory allocator V5.0.1
- Power Management: BIOS and OS set to prefer performance at the cost of additional power usage

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- Max MHz: 3200
- Nominal: 2000
- Enabled: 64 cores, 2 chips, 2 threads/core
- Orderable: 1,2 Chips
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- Storage: 1 x 300 GB 15K SAS HDD
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## SPEC CPU®2017 Floating Point Rate Result

### Cisco Systems

Cisco UCS C240 M6 (Intel Xeon Gold 6338, 2.00GHz)

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### Results Table

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SPECrate®2017_fp_base = 388
SPECrate®2017_fp_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option "submit" was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOCONF = "retain:true"

### General Notes

Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 6338, 2.00GHz)

SPECraten: 2017 fp_base = 388
SPECraten: 2017 fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

General Notes (Continued)

sync; echo 3 > /proc/sys/vm/drop_caches
runcpu command invoked through numacl i.e.:
numacl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
UPI Link Enablement set to l
UPI Power Management set to Enabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDCSparing set to Disabled
Patrol Scrub set to Disabled
Enhanced CPU performance set to Auto
Energy Efficient Turbo set to Enabled
Processor C6 Report set to Enabled
Processor C1E set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acfc64d
running on install Sun Jul 4 07:31:14 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6338 CPU @ 2.00GHz
  2 "physical id"s (chips)
  128 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 32
siblings : 64

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 6338, 2.00GHz)

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Test Date: Jul-2021
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Hardware Availability: Jun-2021
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SPECrate®2017_fp_base = 388
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Platform Notes (Continued)

From lscpu from util-linux 2.33.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 128
On-line CPU(s) list: 0-127
Thread(s) per core: 2
Core(s) per socket: 32
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Gold 6338 CPU @ 2.00GHz
Stepping: 6
CPU MHz: 1248.144
CPU max MHz: 3200.0000
CPU min MHz: 800.0000
BogoMIPS: 4000.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 49152K
NUMA node0 CPU(s): 0-15, 64-79
NUMA node1 CPU(s): 16-31, 80-95
NUMA node2 CPU(s): 32-47, 96-111
NUMA node3 CPU(s): 48-63, 112-127

Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl noalign_tsc paranoid nonstop_tsc cpuid
aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtrunc pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 invpcid_single ssbd
mqa ibrs ibpb stibp ibrs_advanced tpr_shadow vnmi flexpriority ept vpid ept_ad
fsтолб.base tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm rdt_a avx512f
avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha_ni
avx512bw avx512vl xsaveopt xsaves xsavec xgetbv1 xsavec cqm_llc cqm_occup_llc cqm_mbm_total
cqm_mbm_local wbnoinvd dtcim l1d arafi stallgpu pln pts hwp hwp_act_window hwp_epp
hwp_pkg_req avx512vbm umip pku ospke avx512_vbmi2 gfnv vaes vpclmulqdq avx512_vnni
avx512_bitalg tme avx512 vpoptcndq la57 rdpid md_clear pconfug flush_l1d

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 6338, 2.00GHz)

SPECraten\textsuperscript{\textregistered}2017\_fp\_base = 388
SPECraten\textsuperscript{\textregistered}2017\_fp\_peak = Not Run

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</table>

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Platform Notes (Continued)

```
/arch_capabilities

.cache

/proc/cpuinfo

/cache data

cache size : 49152 KB

numactl --hardware

WARNING: a numactl 'node' might or might not correspond to a physical chip.

available: 4 nodes (0-3)

node 0 cpus:  0  1  2  3  4  5  6  7  8  9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63

node 0 size: 257600 MB

node 0 free: 241247 MB

node 1 cpus:  16  17  18  19  20  21  22  23  24  25  26  27  28  29  30  31  32  33  34  35  36  37  38  39  40  41  42  43  44  45  46  47  48  49  50  51  52  53  54  55  56  57  58  59  60  61  62  63

node 1 size: 258040 MB

node 1 free: 244737 MB

node 2 cpus:  32  33  34  35  36  37  38  39  40  41  42  43  44  45  46  47  48  49  50  51  52  53  54  55  56  57  58  59  60  61  62  63  64  65  66  67  68  69  70  71  72  73  74  75

node 2 size: 258040 MB

node 2 free: 245092 MB

node 3 cpus:  48  49  50  51  52  53  54  55  56  57  58  59  60  61  62  63  64  65  66  67  68  69  70  71  72  73  74  75  76  77  78  79  80  81  82  83  84  85  86  87  88

node 3 size: 258036 MB

node 3 free: 244454 MB

node distances:

node 0  1  2  3
0:  10  11  20  20
1:  11  10  20  20
2:  20  20  10  11
3:  20  20  11  10

From /proc/meminfo

MemTotal:       1056478916 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*

os-release:

NAME="SLES"
VERSION="15-SP2"
VERSION_ID="15.2"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
ID="sles"
ID_LIKE="suse"

(Continued on next page)
Platform Notes (Continued)

```plaintext
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp2"
```

uname -a:
```
Linux install 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2018-3639 (Speculative Store Bypass): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs barriers and __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Jul 3 23:04

SPEC is set to: /home/cpu2017
```
Filesystem     Type   Size  Used Avail Use% Mounted on
/dev/sdc2      btrfs  277G   76G  198G  28% /home
```

From /sys/devices/virtual/dmi/id
```
Vendor:        Cisco Systems Inc
Product:       UCSC-C240-M6SX
Serial:        WZP244208SJ
```

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SM BIOS" standard.
```
Memory:
32x 0xCE00 M393A4K40DB3-CWE 32 GB 2 rank 3200

BIOS:
BIOS Vendor:    Cisco Systems, Inc.
BIOS Version:   C240M6.4.2.1c.1.0701210708
BIOS Date:      07/01/2021
BIOS Revision:  5.22
```

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Platform Notes (Continued)

(End of data from sysinfo program)

Compiler Version Notes

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<tr>
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Compiler Version Notes (Continued)

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------------------------------------------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
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Fortran, C | 521.wrf_r(base) 527.cam4_r(base)
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Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
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Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icx

Benchmarks using both C and C++:
icpx icx

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64

(Continued on next page)
SPEC CPU®2017 Floating Point Rate Result

Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 6338, 2.00GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base</th>
<th>388</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_fp_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Jul-2021
Hardware Availability: Jun-2021
Tested by: Cisco Systems
Software Availability: Mar-2021

Base Portability Flags (Continued)

508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

C++ benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Fortran benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
-qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using both Fortran and C:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using both C and C++:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math

(Continued on next page)
Cisco Systems
Cisco UCS C240 M6 (Intel Xeon Gold 6338, 2.00GHz)

SPECrater®2017_fp_base = 388
SPECrater®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Jul-2021
Hardware Availability: Jun-2021
Software Availability: Mar-2021

Base Optimization Flags (Continued)

Benchmarks using both C and C++ (continued):
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using Fortran, C, and C++:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.0-ICX-revF.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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