Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6330, 2.00GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>SPECrate®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>364</td>
<td>377</td>
</tr>
</tbody>
</table>

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems  

<table>
<thead>
<tr>
<th>Hardware</th>
<th>Software</th>
</tr>
</thead>
</table>
| CPU Name: Intel Xeon Gold 6330  
Max MHz: 3100  
Nominal: 2000  
Enabled: 56 cores, 2 chips, 2 threads/core  
Orderable: 1.2 Chips  
Cache L1: 32 KB I + 48 KB D on chip per core  
L2: 1.25 MB I+D on chip per core  
L3: 42 MB I+D on chip per chip  
Other: None  
Memory: 1 TB (32 x 32 GB 2Rx4 PC4-3200V-R, running at 2933)  
Storage: 1 x 300 GB 15K SAS HDD  
Other: None  
| OS: SUSE Linux Enterprise Server 15 SP2  
5.3.18-22-default  
Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux; Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux; C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux  
Parallel: No  
Firmware: Version 4.2.1c released Jul-2021  
File System: btrfs  
System State: Run level 3 (multi-user)  
Base Pointers: 64-bit  
Peak Pointers: 32/64-bit  
Other: jemalloc memory allocator V5.0.1  
Power Management: BIOS and OS set to prefer performance at the cost of additional power usage |

```plaintext
500.perlbench_r 112
502.gcc_r 112
505.mcf_r 112
520.omnetpp_r 112
523.xalancbmk_r 112
525.x264_r 112
531.deepsjeng_r 112
541.leela_r 112
548.exchange2_r 112
557.xz_r 112
```

<table>
<thead>
<tr>
<th>Copies</th>
<th>SPECrate®2017_int_base</th>
<th>SPECrate®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>240</td>
<td>249</td>
</tr>
<tr>
<td>1</td>
<td>253</td>
<td>299</td>
</tr>
<tr>
<td>2</td>
<td>350</td>
<td>624</td>
</tr>
<tr>
<td>3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td></td>
<td></td>
</tr>
<tr>
<td>14</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td></td>
<td></td>
</tr>
<tr>
<td>16</td>
<td></td>
<td></td>
</tr>
<tr>
<td>17</td>
<td></td>
<td></td>
</tr>
<tr>
<td>18</td>
<td></td>
<td></td>
</tr>
<tr>
<td>19</td>
<td></td>
<td></td>
</tr>
<tr>
<td>20</td>
<td></td>
<td></td>
</tr>
<tr>
<td>21</td>
<td></td>
<td></td>
</tr>
<tr>
<td>22</td>
<td></td>
<td></td>
</tr>
<tr>
<td>23</td>
<td></td>
<td></td>
</tr>
<tr>
<td>24</td>
<td></td>
<td></td>
</tr>
<tr>
<td>25</td>
<td></td>
<td></td>
</tr>
<tr>
<td>26</td>
<td></td>
<td></td>
</tr>
<tr>
<td>27</td>
<td></td>
<td></td>
</tr>
<tr>
<td>28</td>
<td></td>
<td></td>
</tr>
<tr>
<td>29</td>
<td></td>
<td></td>
</tr>
<tr>
<td>30</td>
<td></td>
<td></td>
</tr>
<tr>
<td>31</td>
<td></td>
<td></td>
</tr>
<tr>
<td>32</td>
<td></td>
<td></td>
</tr>
<tr>
<td>33</td>
<td></td>
<td></td>
</tr>
<tr>
<td>34</td>
<td></td>
<td></td>
</tr>
<tr>
<td>35</td>
<td></td>
<td></td>
</tr>
<tr>
<td>36</td>
<td></td>
<td></td>
</tr>
<tr>
<td>37</td>
<td></td>
<td></td>
</tr>
<tr>
<td>38</td>
<td></td>
<td></td>
</tr>
<tr>
<td>39</td>
<td></td>
<td></td>
</tr>
<tr>
<td>40</td>
<td></td>
<td></td>
</tr>
<tr>
<td>41</td>
<td></td>
<td></td>
</tr>
<tr>
<td>42</td>
<td></td>
<td></td>
</tr>
<tr>
<td>43</td>
<td></td>
<td></td>
</tr>
<tr>
<td>44</td>
<td></td>
<td></td>
</tr>
<tr>
<td>45</td>
<td></td>
<td></td>
</tr>
<tr>
<td>46</td>
<td></td>
<td></td>
</tr>
<tr>
<td>47</td>
<td></td>
<td></td>
</tr>
<tr>
<td>48</td>
<td></td>
<td></td>
</tr>
<tr>
<td>49</td>
<td></td>
<td></td>
</tr>
<tr>
<td>50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>51</td>
<td></td>
<td></td>
</tr>
<tr>
<td>52</td>
<td></td>
<td></td>
</tr>
<tr>
<td>53</td>
<td></td>
<td></td>
</tr>
<tr>
<td>54</td>
<td></td>
<td></td>
</tr>
<tr>
<td>55</td>
<td></td>
<td></td>
</tr>
<tr>
<td>56</td>
<td></td>
<td></td>
</tr>
<tr>
<td>57</td>
<td></td>
<td></td>
</tr>
<tr>
<td>58</td>
<td></td>
<td></td>
</tr>
<tr>
<td>59</td>
<td></td>
<td></td>
</tr>
<tr>
<td>60</td>
<td></td>
<td></td>
</tr>
<tr>
<td>61</td>
<td></td>
<td></td>
</tr>
<tr>
<td>62</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63</td>
<td></td>
<td></td>
</tr>
<tr>
<td>64</td>
<td></td>
<td></td>
</tr>
<tr>
<td>65</td>
<td></td>
<td></td>
</tr>
<tr>
<td>66</td>
<td></td>
<td></td>
</tr>
<tr>
<td>67</td>
<td></td>
<td></td>
</tr>
<tr>
<td>68</td>
<td></td>
<td></td>
</tr>
<tr>
<td>69</td>
<td></td>
<td></td>
</tr>
<tr>
<td>70</td>
<td></td>
<td></td>
</tr>
<tr>
<td>71</td>
<td></td>
<td></td>
</tr>
<tr>
<td>72</td>
<td></td>
<td></td>
</tr>
<tr>
<td>73</td>
<td></td>
<td></td>
</tr>
<tr>
<td>74</td>
<td></td>
<td></td>
</tr>
<tr>
<td>75</td>
<td></td>
<td></td>
</tr>
<tr>
<td>76</td>
<td></td>
<td></td>
</tr>
<tr>
<td>77</td>
<td></td>
<td></td>
</tr>
<tr>
<td>78</td>
<td></td>
<td></td>
</tr>
<tr>
<td>79</td>
<td></td>
<td></td>
</tr>
<tr>
<td>80</td>
<td></td>
<td></td>
</tr>
<tr>
<td>81</td>
<td></td>
<td></td>
</tr>
<tr>
<td>82</td>
<td></td>
<td></td>
</tr>
<tr>
<td>83</td>
<td></td>
<td></td>
</tr>
<tr>
<td>84</td>
<td></td>
<td></td>
</tr>
<tr>
<td>85</td>
<td></td>
<td></td>
</tr>
<tr>
<td>86</td>
<td></td>
<td></td>
</tr>
<tr>
<td>87</td>
<td></td>
<td></td>
</tr>
<tr>
<td>88</td>
<td></td>
<td></td>
</tr>
<tr>
<td>89</td>
<td></td>
<td></td>
</tr>
<tr>
<td>90</td>
<td></td>
<td></td>
</tr>
<tr>
<td>91</td>
<td></td>
<td></td>
</tr>
<tr>
<td>92</td>
<td></td>
<td></td>
</tr>
<tr>
<td>93</td>
<td></td>
<td></td>
</tr>
<tr>
<td>94</td>
<td></td>
<td></td>
</tr>
<tr>
<td>95</td>
<td></td>
<td></td>
</tr>
<tr>
<td>96</td>
<td></td>
<td></td>
</tr>
<tr>
<td>97</td>
<td></td>
<td></td>
</tr>
<tr>
<td>98</td>
<td></td>
<td></td>
</tr>
<tr>
<td>99</td>
<td></td>
<td></td>
</tr>
<tr>
<td>100</td>
<td></td>
<td></td>
</tr>
<tr>
<td>101</td>
<td></td>
<td></td>
</tr>
<tr>
<td>102</td>
<td></td>
<td></td>
</tr>
<tr>
<td>103</td>
<td></td>
<td></td>
</tr>
<tr>
<td>104</td>
<td></td>
<td></td>
</tr>
<tr>
<td>105</td>
<td></td>
<td></td>
</tr>
<tr>
<td>106</td>
<td></td>
<td></td>
</tr>
<tr>
<td>107</td>
<td></td>
<td></td>
</tr>
<tr>
<td>108</td>
<td></td>
<td></td>
</tr>
<tr>
<td>109</td>
<td></td>
<td></td>
</tr>
<tr>
<td>110</td>
<td></td>
<td></td>
</tr>
<tr>
<td>111</td>
<td></td>
<td></td>
</tr>
<tr>
<td>112</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```
Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>112</td>
<td>717</td>
<td>249</td>
<td>717</td>
<td>249</td>
<td>718</td>
<td>248</td>
<td>717</td>
<td>249</td>
<td>718</td>
<td>248</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>112</td>
<td>530</td>
<td>299</td>
<td>529</td>
<td>300</td>
<td>531</td>
<td>299</td>
<td>529</td>
<td>300</td>
<td>531</td>
<td>299</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>112</td>
<td>290</td>
<td>624</td>
<td>290</td>
<td>624</td>
<td>290</td>
<td>624</td>
<td>290</td>
<td>624</td>
<td>290</td>
<td>624</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>112</td>
<td>644</td>
<td>228</td>
<td>644</td>
<td>228</td>
<td>646</td>
<td>228</td>
<td>644</td>
<td>228</td>
<td>646</td>
<td>228</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>112</td>
<td>258</td>
<td>459</td>
<td>257</td>
<td>460</td>
<td>257</td>
<td>461</td>
<td>258</td>
<td>459</td>
<td>257</td>
<td>461</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>112</td>
<td>261</td>
<td>751</td>
<td>261</td>
<td>751</td>
<td>261</td>
<td>751</td>
<td>261</td>
<td>751</td>
<td>261</td>
<td>751</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>112</td>
<td>470</td>
<td>273</td>
<td>471</td>
<td>273</td>
<td>471</td>
<td>273</td>
<td>470</td>
<td>273</td>
<td>471</td>
<td>273</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>112</td>
<td>691</td>
<td>268</td>
<td>692</td>
<td>268</td>
<td>692</td>
<td>268</td>
<td>691</td>
<td>268</td>
<td>692</td>
<td>268</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>112</td>
<td>398</td>
<td>737</td>
<td>399</td>
<td>736</td>
<td>400</td>
<td>734</td>
<td>398</td>
<td>737</td>
<td>399</td>
<td>736</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>112</td>
<td>584</td>
<td>207</td>
<td>586</td>
<td>207</td>
<td>586</td>
<td>206</td>
<td>582</td>
<td>204</td>
<td>593</td>
<td>204</td>
</tr>
</tbody>
</table>

SPECrate®2017_int_base = 364
SPECrate®2017_int_peak = 377

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH =
"/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

MALLOC_CONF = "retain:true"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesyste page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6330, 2.00GHz)  

SPEC CPU®2017 Integer Rate Result
Copyright 2017-2021 Standard Performance Evaluation Corporation

SPECrater®2017_int_base = 364
SPECrater®2017_int_peak = 377

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Jul-2021
Hardware Availability: Apr-2021
Software Availability: Mar-2021

General Notes (Continued)
runccpu command invoked through numactl i.e.:
numactl --interleave=all runccpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes
BIOS Settings:
Adjacent Cache Line Prefetcher set to Disabled
DCU Streamer Prefetch set to Disabled
UPI Link Enablement set to 1
UPI Power Management set to Enabled
Sub NUMA Clustering set to Enabled
LLC Dead Line set to Disabled
Memory Refresh Rate set to 1x Refresh
ADDDC Sparing set to Disabled
Patrol Scrub set to Disabled
Enhanced CPU performance set to Auto
Energy Efficient Turbo set to Enabled
Processor C6 Report set to Enabled
Processor C1E set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d running on localhost Mon Jul 12 02:08:38 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6330 CPU @ 2.00GHz
          2  "physical id"s (chips)
          112 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 28
siblings : 56
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6330, 2.00GHz)

SPECrate®2017_int_base = 364
SPECrate®2017_int_peak = 377

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jul-2021
Hardware Availability: Apr-2021
Software Availability: Mar-2021

Platform Notes (Continued)

25 26 27
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
25 26 27

From lscpu from util-linux 2.33.1:
Architecture:        x86_64
CPU op-mode(s):      32-bit, 64-bit
Byte Order:          Little Endian
Address sizes:       46 bits physical, 57 bits virtual
CPU(s):              112
On-line CPU(s) list: 0-111
Thread(s) per core:  2
Core(s) per socket:  28
Socket(s):           2
NUMA node(s):        4
Vendor ID:           GenuineIntel
CPU family:          6
Model:               106
Model name:          Intel(R) Xeon(R) Gold 6330 CPU @ 2.00GHz
Stepping:            6
CPU MHz:             2600.000
CPU max MHz:         3100.0000
CPU min MHz:         800.0000
BogoMIPS:            4000.00
Virtualization:      VT-x
L1d cache:           48K
L1i cache:           32K
L2 cache:            1280K
L3 cache:            43008K
NUMA node0 CPU(s):   0-13,56-69
NUMA node1 CPU(s):   14-27,70-83
NUMA node2 CPU(s):   28-41,84-97
NUMA node3 CPU(s):   42-55,98-111
Flags:               fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpref pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtrr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invpcid_single ssbd
mba ibrs ibrd ibrs_enhanced tpr_shadow vnmi flexpriority ept vpid ept_ad
fsibase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm rdt_a avx512f
avx512dq rsrdsd adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha ni
avx512bw avx512vl xsaveopt xsaves xsavec xsaves cqm_llc cqm_occup_llc cqm_mbm_total
cqm_mbm_local wbnoinvd dtherm ida arat pln pts hwp hwp_act_window hwp_epp
hwp_pkg_req avx512vmbi umip pku ospke avx512_vmbi2 gfnq vaes vpclmulqdq avx512_vnni
avx512_bitalg tme avx512_vpopcntdq la57 rdrpid md_clear pconfcl flush llid
arch_capabilities

(Continued on next page)
Platform Notes (Continued)

/proc/cpuinfo cache data
   cache size : 43008 KB

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
   available: 4 nodes (0-3)
   node 0 cpus:  0  1  2  3  4  5  6  7  8  9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 70 71 72 73 74 75 76 77 78 79 80 81 82 83
   node 0 size:   257562 MB
   node 0 free:   257059 MB
   node 1 cpus: 14 15 16 17 18 19 20 21 22 23 24 25 26 27 70 71 72 73 74 75 76 77 78 79 80 81 82 83
   node 1 size:   258007 MB
   node 1 free:   257594 MB
   node 2 cpus: 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 98 99 100 101 102 103 104 105 106 107 108 109 110 111
   node 2 size:   258041 MB
   node 2 free:   257748 MB
   node 3 cpus: 42 43 44 45 46 47 48 49 50 51 52 53 54 55 98 99 100 101 102 103 104 105
   node 3 size:   257763 MB
   node 3 free:   257457 MB
   node distances:
   node   0   1   2   3
   0:  10  11  20  20
   1:  11  20  20  20
   2:  20  20  10  11
   3:  20  20  11  10

From /proc/meminfo
   MemTotal:        1056127492 kB
   HugePages_Total:       0
   Hugepagesize:            2048 kB

/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release* /etc/*version*
   os-release:
      NAME="SLES"
      VERSION="15-SP2"
      VERSION_ID="15.2"
      PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
      ID="sles"
      ID_LIKE="suse"
      ANSI_COLOR="0;32"
      CPE_NAME="cpe:/o:suse:sles:15:sp2"
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6330, 2.00GHz)

SPEC CPU®2017 Integer Rate Result

SPECrated2017_int_base = 364
SPECrated2017_int_peak = 377

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jul-2021
Hardware Availability: Apr-2021
Software Availability: Mar-2021

Platform Notes (Continued)

uname -a:
    Linux localhost 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
    x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Mitigation: Speculative Store
CVE-2018-3639 (Speculative Store Bypass): Bypass disabled via prctl and
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs
CVE-2017-5715 (Spectre variant 2): barriers and __user pointer
CVE-2020-0543 (Special Register Buffer Data Sampling): sanitation
CVE-2019-11135 (TSX Asynchronous Abort): Mitigation: Enhanced IBRS, IBPB:
run-level 3 Jul 12 01:39
conditional, RSB filling
SPEC is set to: /home/cpu2017
From /sys/devices/virtual/dmi/id
Vendor: Cisco Systems Inc
Product: UCSC-C220-M6S
Serial: WZP24430N7F

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you
interpret this section. The 'dmidecode' program reads system data which is "intended to
allow hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
    32x 0xCE00 M393A4K40DB3-CWE 32 GB 2 rank 3200, configured at 2933

BIOS:
    BIOS Vendor: Cisco Systems, Inc.
    BIOS Version: C220M6.4.2.1c.1.0701210708
    BIOS Date: 07/01/2021
    BIOS Revision: 5.22

(End of data from sysinfo program)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6330, 2.00GHz)

SPECrate®2017_int_base = 364
SPECrate®2017_int_peak = 377

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jul-2021
Hardware Availability: Apr-2021
Software Availability: Mar-2021

Compiler Version Notes

==============================================================================
| C       | 500.perlbench_r(peak) 557.xz_r(peak)
|---------|-------------------------------------------------------------------------
| Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
| Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
|---------|-------------------------------------------------------------------------

==============================================================================
| C       | 502.gcc_r(peak)
|---------|-------------------------------------------------------------------------
| Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version 2021.1 Build 20201113
| Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
|---------|-------------------------------------------------------------------------

==============================================================================
| C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
|---------|-------------------------------------------------------------------------
| 525.x264_r(base, peak) 557.xz_r(base)
| Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
| Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
|---------|-------------------------------------------------------------------------

==============================================================================
| C       | 500.perlbench_r(peak) 557.xz_r(peak)
|---------|-------------------------------------------------------------------------
| Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
| Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
|---------|-------------------------------------------------------------------------

==============================================================================
| C       | 502.gcc_r(peak)
|---------|-------------------------------------------------------------------------
| Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version 2021.1 Build 20201113
| Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
|---------|-------------------------------------------------------------------------

==============================================================================
| C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
|---------|-------------------------------------------------------------------------
| 525.x264_r(base, peak) 557.xz_r(base)
| Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
| (Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6330, 2.00GHz)

SPEC CPU®2017 Integer Rate Result
Copyright 2017-2021 Standard Performance Evaluation Corporation

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Hardware Availability: Apr-2021
Test Date: Jul-2021
Tested by: Cisco Systems
Software Availability: Mar-2021

Compiler Version Notes (Continued)

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

perlbench_r(peak) xz_r(peak)

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

gcc_r(peak)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on IA-32, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

perlbench_r(base) gcc_r(base) mcf_r(base, peak)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

omnetpp_r(base, peak) xalancbmk_r(base, peak)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

omnetpp_r(base, peak) xalancbmk_r(base, peak)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

exchange2_r(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
## Base Compiler Invocation

C benchmarks:
- icx

C++ benchmarks:
- icpx

Fortran benchmarks:
- ifort

## Base Portability Flags

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Flags</th>
</tr>
</thead>
<tbody>
<tr>
<td>perlbench_r</td>
<td>-DSPEC_LP64 -DSPEC_LINUX_X64</td>
</tr>
<tr>
<td>gcc_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>mcf_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>omnetpp_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>xalancbmk_r</td>
<td>-DSPEC_LP64 -DSPEC_LINUX</td>
</tr>
<tr>
<td>x264_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>deepsjeng_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>leela_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>exchange2_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>xz_r</td>
<td>-DSPEC_LP64</td>
</tr>
</tbody>
</table>

## Base Optimization Flags

C benchmarks:
- \(-w \-std=\text{c11} \-m64 \-Wl,\-z,\text{muldefs} \-xCORE-AVX512 \-O3 \-ffast-math \-flto \-mfpmath=\text{sse} \-funroll-loops \-qopt-mem-layout-trans=4 \-mbranches-within-32B-boundaries \-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin \-Lqkmalloc |

C++ benchmarks:
- \(-w \-m64 \-Wl,\-z,\text{muldefs} \-xCORE-AVX512 \-O3 \-ffast-math \-flto \-mfpmath=\text{sse} \-funroll-loops \-qopt-mem-layout-trans=4 \-mbranches-within-32B-boundaries \-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin \-Lqkmalloc |

Fortran benchmarks:
- \(-w \-m64 \-Wl,\-z,\text{muldefs} \-xCORE-AVX512 \-O3 \-ipo \-no-prec-div \-qopt-mem-layout-trans=4 \-nostandard-realloc-lhs \-align array32byte \-auto \-mbranches-within-32B-boundaries |

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6330, 2.00GHz)

SPEC CPU®2017 Integer Rate Result
Copyright 2017-2021 Standard Performance Evaluation Corporation

SPECrate®2017_int_base = 364
SPECrate®2017_int_peak = 377

Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6330, 2.00GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Jul-2021
Hardware Availability: Apr-2021
Software Availability: Mar-2021

Base Optimization Flags (Continued)
Fortran benchmarks (continued):
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

Peak Compiler Invocation
C benchmarks (except as noted below):
icx

500.perlbench_r: icc
557.xz_r: icc

C++ benchmarks:
icpx
Fortran benchmarks:
ifort

Peak Portability Flags
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags
C benchmarks:
500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)
-xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-strict-overflow
-mbranches-within-32B-boundaries

(Continued on next page)
Cisco Systems
Cisco UCS C220 M6 (Intel Xeon Gold 6330, 2.00GHz)

Peak Optimization Flags (Continued)

500.perlbench r (continued):
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

502.gcc_r: -m32
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/ia32_lin
-std=gnu89 -Wl,-z,muldefs -fprofile-generate(pass1)
-fprofile-use=default.profdata(pass 2) -xCORE-AVX512 -flto
-Ofast(pass1) -O3 -ffast-math -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/usr/local/jemalloc32-5.0.1/lib -ljemalloc

505.mcf_r: basepeak = yes

525.x264_r: -w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -flto
-O3 -ffast-math -qopt-mem-layout-trans=4 -fno-alias
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

557.xz_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin
-lqkmalloc

C++ benchmarks:

520.omnetpp_r: basepeak = yes

523.xalancbmk_r: basepeak = yes

531.deepsjeng_r: basepeak = yes

541.leela_r: basepeak = yes

Fortran benchmarks:

548.exchange2_r: basepeak = yes

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.0-ICX-revF.xml
### SPEC CPU®2017 Integer Rate Result

**Cisco Systems**
Cisco UCS C220 M6 (Intel Xeon Gold 6330, 2.00GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>364</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_int_peak</td>
<td>377</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Test Date:</td>
<td>Jul-2021</td>
</tr>
<tr>
<td>Hardware Availability:</td>
<td>Apr-2021</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>Mar-2021</td>
</tr>
</tbody>
</table>

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.8 on 2021-07-12 05:08:37-0400.
Report generated on 2021-08-04 18:20:26 by CPU2017 PDF formatter v6442.
Originally published on 2021-08-04.