Hewlett Packard Enterprise
(Test Sponsor: HPE)
ProLiant DL360 Gen10 Plus
(2.30 GHz, Intel Xeon Gold 6314U)

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Test Date: Jul-2021
Hardware Availability: Jun-2021
Software Availability: Dec-2020

<table>
<thead>
<tr>
<th>SPECuerspec2017_fp_base</th>
<th>SPECuerspec2017_fp_peak</th>
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<tr>
<td>137</td>
<td>140</td>
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 Threads

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<tr>
<th>603.bwaves_s</th>
<th>32</th>
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<tr>
<td>607.cactuBSSN_s</td>
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<tr>
<td>619.ibm_s</td>
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<td>644.nab_s</td>
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<td>649.fotonik3d_s</td>
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<td>654.roms_s</td>
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</table>

 SPECuerspec2017_fp_base (137) SPECuerspec2017_fp_peak (140)

 Software

OS: Red Hat Enterprise Linux 8.3 (Ootpa)
Kernel 4.18.0-240.el8.x86_64

Compiler:
C/C++: Version 2021.1 of Intel oneAPI DPC++/C++
Compiler Build 20201113 for Linux;
Fortran: Version 2021.1 of Intel Fortran Compiler
Classic Build 20201112 for Linux;
C/C++: Version 2021.1 of Intel C/C++ Compiler
Classic Build 20201112 for Linux

Parallel: Yes
Firmware: HPE BIOS Version U46 v1.42 05/26/2021 released
May-2021
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS set to prefer performance at the cost of additional power usage

Hardware

CPU Name: Intel Xeon Gold 6314U
Max MHz: 3400
Nominal: 2300
Enabled: 32 cores, 1 chip
Orderable: 1, 2 chip(s)
Cache L1: 32 KB I + 48 KB D on chip per core
L2: 1.25 MB I+D on chip per core
L3: 48 MB I+D on chip per chip
Other: None
Memory: 1 TB (16 x 64 GB 2Rx4 PC4-3200AA-R)
Storage: 1 x 800 GB SAS SSD, RAID 0
Other: None
SPEC CPU®2017 Floating Point Speed Result

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ProLiant DL360 Gen10 Plus
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SPECspeed®2017_fp_base = 137
SPECspeed®2017_fp_peak = 140

Results Table

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<tr>
<th>Benchmark</th>
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</tbody>
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SPECspeed®2017_fp_base = 137
SPECspeed®2017_fp_peak = 140

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
    sync; echo 3> /proc/sys/vm/drop_caches

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOC_CONF = "retain:true"
OMP_STACKSIZE = "192M"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM memory using Redhat Enterprise Linux 8.0
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

(Continued on next page)
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SPECspeed\textsuperscript{®}2017\_fp\_peak = 140
SPECspeed\textsuperscript{®}2017\_fp\_base = 137

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

General Notes (Continued)


Submitted by: "Bhatnagar, Prateek" <prateek.bhatnagar@hpe.com>
Submitted: Mon Jul 19 06:09:43 EDT 2021
Submission: cpu2017-20210719-28204.sub

Platform Notes

The system ROM used for this result contains Intel microcode version 0xd0002a0 for the Intel Xeon Gold 6314U processor

BIOS Configuration:
Workload Profile set to General Peak Frequency Compute
Intel Hyper-Threading set to Disabled
Thermal Configuration set to Maximum Cooling
Memory Patrol Scrubbing set to Disabled
Advanced Memory Protection set to Advanced ECC
Last Level Cache (LLC) Prefetch set to Enabled
Last Level Cache (LLC) Dead Line Allocation set to Disabled
Enhanced Processor Performance set to Enabled
Workload Profile set to Custom
  Energy/Performance Bias set to Balanced Power
  DCU Stream Prefetcher set to Disabled
  Adjacent Sector Prefetch set to Disabled
  Minimum Processor Idle Power Package C-State set to No Package State
  Numa Group Size Optimization set to Flat

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16aca664d
running on localhost.localdomain Wed Jul 14 15:07:08 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
  model name : Intel(R) Xeon(R) Gold 6314U CPU @ 2.30GHz
  1 "physical id"s (chips)
  32 "processors"
  cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 32
  siblings : 32
  physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31

From lscpu from util-linux 2.32.1:

(Continued on next page)
Hewlett Packard Enterprise
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SPECspeed®2017_fp_base = 137
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Test Date: Jul-2021
Hardware Availability: Jun-2021
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Platform Notes (Continued)

Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 32
On-line CPU(s) list: 0-31
Thread(s) per core: 1
Core(s) per socket: 32
Socket(s): 1
NUMA node(s): 1
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Gold 6314U CPU @ 2.30GHz
Stepping: 6
CPU MHz: 1414.922
BogoMIPS: 4600.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 49152K
NUMA node0 CPU(s): 0-31
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpref pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 invpcid_single ssbd
mba ibrs stibp ibrs_enhanced tpr_shadow vni flexpriority ept vpid ept_ad
fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ibrms invpcid cqm rdtscp
AVX RDSEED ADX SMAP AVX512IFMA CLFLUSHOPT CLWB INTEL_PT AVX512CD SHA_NI AVX512BW
AVX512VL XSAVEOPT XSAVE XCACHE XGETBV1 XSAVE CQMM_MC_CQM_OCCUP_11C CQM_MBM_TOTAL
CQM_MBM_LOCAL SPLIT_LOCK_DETECT WHBOINVD DTHERM IDA ARAT PLN PTS AVX512VBM1 UMPI PU
OSPKA AVX512_VBM12 GFNI VAES VPCLMULQDQ AVX512_VNNI AVX512_BITALG TME
AVX512_VPOPCNTDQ LA57 RDPID MD_CLEAR PCONFIG FLUSH_L1D ARCH_CAPABILITIES

/proc/cpuinfo cache data
  cache size : 49152 KB

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 1 nodes (0)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27
  28 29 30 31
  node 0 size: 965616 MB
  node 0 free: 1023973 MB
  node distances:
SPEC CPU®2017 Floating Point Speed Result

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SPECspeed®2017_fp_base = 137
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CPU2017 License: 3
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<td>Jul-2021</td>
<td>Jun-2021</td>
<td>Dec-2020</td>
</tr>
</tbody>
</table>

Platform Notes (Continued)

node 0
0: 10

From /proc/meminfo
MemTotal: 1056532732 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/sbin/tuned-adm active
Current active profile: throughput-performance

From /etc/*release* /etc/*version*
os-release:
NAME="Red Hat Enterprise Linux"
VERSION="8.3 (Ootpa)"
ID="rhel"
ID_LIKE="fedora"
VERSION_ID="8.3"
PLATFORM_ID="platform:el8"
PRETTY_NAME="Red Hat Enterprise Linux 8.3 (Ootpa)"
ANSI_COLOR="0;31"
redhat-release: Red Hat Enterprise Linux release 8.3 (Ootpa)
system-release: Red Hat Enterprise Linux release 8.3 (Ootpa)
system-release-cpe: cpe:/o:redhat:enterprise_linux:8.3:ga
uname -a:
Linux localhost.localdomain 4.18.0-240.el8.x86_64 #1 SMP Wed Sep 23 05:13:10 EDT 2020
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swaps barriers and __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Jul 14 10:51

(Continued on next page)
SPEC CPU®2017 Floating Point Speed Result

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 SPECspeed®2017_fp_base = 137
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Platform Notes (Continued)

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/mapper/rhel-home xfs 670G 111G 559G 17% /home

From /sys/devices/virtual/dmi/id
Vendor: HPE
Product: ProLiant DL360 Gen10 Plus
Product Family: ProLiant
Serial: CN7013030H

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
16x Micron 36ASF8G72PZ-3G2B2 64 GB 2 rank 3200
16x UNKNOWN NOT AVAILABLE

BIOS:
BIOS Vendor: HPE
BIOS Version: U46
BIOS Date: 05/26/2021
BIOS Revision: 1.42
Firmware Revision: 2.42

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
| C | 619.lbm_s(base, peak) 638.imagick_s(base, peak) 644.nab_s(base) |
==============================================================================

----------------------------- Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
-----------------------------

----------------------------- Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
-----------------------------

(Continued on next page)
## Compiler Version Notes (Continued)

```plaintext
C               | 619.lbm_s(base, peak) 638.imagick_s(base, peak)
                | 644.nab_s(base)

Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

C               | 644.nab_s(peak)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

C++, C, Fortran | 607.cactuBSSN_s(base, peak)

Intel(R) C++ Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Fortran         | 603.bwaves_s(base, peak) 649.fotonik3d_s(base, peak)
                | 654.roms_s(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Fortran, C      | 621.wrf_s(base, peak) 627.cam4_s(base, peak)
                | 628.pop2_s(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
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Copyright 2017-2021 Standard Performance Evaluation Corporation

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Compiler Version Notes (Continued)

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Intel (R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactusBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-m64 -std=c11 -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-mbranches-within-32B-boundaries

(Continued on next page)
## SPEC CPU®2017 Floating Point Speed Result

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**CPU2017 License:** 3  
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**Tested by:** HPE

**Test Date:** Jul-2021  
**Hardware Availability:** Jun-2021  
**Software Availability:** Dec-2020

### Base Optimization Flags (Continued)

- Fortran benchmarks:
  -m64 -Wl,-z,muldefs -DSPEC_OPENMP -xCORE-AVX512 -ipo -O3  
  -no-prec-div -qopt-prefetch    -ffinite-math-only  
  -qopt-mem-layout-trans=4 -qopenmp -nostandard-realloc-lhs  
  -mbranches-within-32B-boundaries -L/usr/local/jemalloc64-5.0.1/lib  
  -ljemalloc

- Benchmarks using both Fortran and C:
  -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
  -qopt-prefetch    -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp  
  -DSPEC_OPENMP -mbranches-within-32B-boundaries -nostandard-realloc-lhs  
  -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

- Benchmarks using Fortran, C, and C++:
  -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
  -qopt-prefetch    -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp  
  -DSPEC_OPENMP -mbranches-within-32B-boundaries -nostandard-realloc-lhs  
  -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

### Peak Compiler Invocation

- C benchmarks (except as noted below):
  - icc

- 644.nab_s: icx

- Fortran benchmarks:
  - ifort

- Benchmarks using both Fortran and C:
  - ifort icc

- Benchmarks using Fortran, C, and C++:
  - icpc icc ifort

### Peak Portability Flags

Same as Base Portability Flags
**SPEC CPU®2017 Floating Point Speed Result**

**Hewlett Packard Enterprise**  
(Test Sponsor: HPE)  
ProLiant DL360 Gen10 Plus  
(2.30 GHz, Intel Xeon Gold 6314U)  

<table>
<thead>
<tr>
<th>SPECspeed®2017_fp_base = 137</th>
<th>SPECspeed®2017_fp_peak = 140</th>
</tr>
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<tr>
<td>CPU2017 License: 3</td>
<td>Test Date:</td>
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<td>Hardware Availability: Jun-2021</td>
</tr>
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<td>Tested by: HPE</td>
<td>Software Availability: Dec-2020</td>
</tr>
</tbody>
</table>

### Peak Optimization Flags

**C benchmarks:**

- `619.lbm_s`: `basepeak = yes`

- `638.imagick_s`: `basepeak = yes`


**Fortran benchmarks:**

- `603.bwaves_s`: `-m64 -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -DSPEC_SUPPRESS_OPENMP -DSPEC_OPENMP -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -nostandard-realloc-lhs -mbranches-within-32B-boundaries -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc`

- `649.fotonik3d_s`: Same as 603.bwaves_s

- `654.roms_s`: `basepeak = yes`

**Benchmarks using both Fortran and C:**

- `621.wrf_s`: `-m64 -std=c11 -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP -mbranches-within-32B-boundaries -nostandard-realloc-lhs -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc`

- `627.cam4_s`: `basepeak = yes`

- `628.pop2_s`: `basepeak = yes`

**Benchmarks using Fortran, C, and C++:**

- `607.cactuBSSN_s`: `basepeak = yes`
### SPEC CPU®2017 Floating Point Speed Result

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The flags files that were used to format this result can be browsed at  
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.0-ICX-revE.html  

You can also download the XML flags sources by saving the following links:  
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.0-ICX-revE.xml  
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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