## Dell Inc.

PowerEdge R750 (Intel Xeon Silver 4310T, 2.30 GHz)

<table>
<thead>
<tr>
<th>SPEC CPU®2017 Floating Point Rate Result</th>
<th>Dell Inc.</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>CPU2017 License:</strong> 55</td>
<td>Dell Inc.</td>
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<tr>
<td><strong>Test Sponsor:</strong> Dell Inc.</td>
<td>Dell Inc.</td>
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<td><strong>Test Date:</strong> Jun-2021</td>
<td>Dell Inc.</td>
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<tr>
<td><strong>Hardware Availability:</strong> May-2021</td>
<td>Dell Inc.</td>
</tr>
<tr>
<td><strong>Software Availability:</strong> Feb-2021</td>
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</tr>
<tr>
<td><strong>SPECrate®2017_fp_base = 170</strong></td>
<td>Dell Inc.</td>
</tr>
<tr>
<td><strong>SPECrate®2017_fp_peak = 175</strong></td>
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</tr>
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<tr>
<th>Copies</th>
<th>SPECrate®2017_fp_base (170)</th>
<th>SPECrate®2017_fp_peak (175)</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>507.caCTuBSSN_r</td>
<td>508.namd_r</td>
</tr>
<tr>
<td>40</td>
<td>108</td>
<td>95.7</td>
</tr>
<tr>
<td>510.parest_r</td>
<td>511.povray_r</td>
<td>519.lbM_r</td>
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<tr>
<td>40</td>
<td>105</td>
<td>143</td>
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<tr>
<td>521.wrf_r</td>
<td>526.blender_r</td>
<td>527.cam4_r</td>
</tr>
<tr>
<td>40</td>
<td>149</td>
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</tr>
<tr>
<td>528.imagick_r</td>
<td>544.nab_r</td>
<td>549.fotonik3d_r</td>
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<td>40</td>
<td>244</td>
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<td>554.roms_r</td>
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<tr>
<td>40</td>
<td>79.9</td>
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</tbody>
</table>

---

### Hardware

- **CPU Name:** Intel Xeon Silver 4310T
- **Max MHz:** 3400
- **Nominal:** 2300
- **Enabled:** 20 cores, 2 chips, 2 threads/core
- **Orderable:** 1.2 chips
- **Cache L1:** 32 KB I + 48 KB D on chip per core
- **L2:** 1.25 MB I+D on chip per core
- **L3:** 15 MB I+D on chip per core
- **Other:** None
- **Memory:** 512 GB (16 x 32 GB 2Rx8 PC4-3200AA-R, running at 2666)
- **Storage:** 225 GB on tmpfs
- **Other:** None

### Software

- **OS:** Red Hat Enterprise Linux 8.3 (Ootpa) 4.18.0-240.15.1.el8_3.x86_64
- **Compiler:** C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux; Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux; C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux
- **Parallel:** No
- **Firmware:** Version 1.2.1 released May-2021
- **File System:** tmpfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 64-bit
- **Other:** jemalloc memory allocator V5.0.1
- **Power Management:** BIOS and OS set to prefer performance at the cost of additional power usage.
## Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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</tr>
</tbody>
</table>

SpecRat®2017_fp_base = 170
SpecRat®2017_fp_peak = 175

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:

LD_LIBRARY_PATH = 
"/mnt/ramdisk2/cpu2017-1.1.5-ic2021.1/lib/intel64:/mnt/ramdisk2/cpu2017-1.1.5-ic2021.1/je5.0.1-64"

MALLOC_CONF = "retain:true"

### General Notes

Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM memory using Red Hat Enterprise Linux 8.1
Transparent Huge Pages enabled by default

(Continued on next page)
Dell Inc. PowerEdge R750 (Intel Xeon Silver 4310T, 2.30 GHz)

SPECrate®2017_fp_base = 170
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CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

General Notes (Continued)

Prior to runcpu invocation
Filesystem page cache synced and cleared with:
   sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
   numactl --interleave=all runcpu <etc>
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.

Benchmark run from a 225 GB ramdisk created with the cmd: ”mount -t tmpfs -o size=225G tmpfs /mnt/ramdisk”

Platform Notes

BIOS Settings:
   Sub NUMA Cluster : 2-Way Clustering
   Virtualization Technology : Disabled

   System Profile : Custom
   CPU Power Management : Maximum Performance
   C1E : Disabled
   C States : Autonomous
   Memory Patrol Scrub : Disabled
   Energy Efficiency Policy : Performance
   CPU Interconnect Bus Link
     Power Management : Disabled
   PCI ASPM L1 Link
     Power Management : Disabled

Sysinfo program /mnt/ramdisk2/cpu2017-1.1.5-ic2021.1/bin/sysinfo
Rev: r6538 of 2020-09-24 e8664e66d2d7080afeaa89d4b38e2f1c
running on localhost.localdomain Fri Jun 11 18:23:57 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
   https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
   model name : Intel(R) Xeon(R) Silver 4310T CPU @ 2.30GHz

(Continued on next page)
### Platform Notes (Continued)

2 "physical id"s (chips)  
40 "processors"

cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

- cpu cores : 10
- siblings : 20
- physical 0: cores 0 1 2 3 4 5 6 7 8 9
- physical 1: cores 0 1 2 3 4 5 6 7 8 9

From lscpu:
- Architecture: x86_64
- CPU op-mode(s): 32-bit, 64-bit
- Byte Order: Little Endian
- CPU(s): 40
- On-line CPU(s) list: 0-39
- Thread(s) per core: 2
- Core(s) per socket: 10
- Socket(s): 2
- NUMA node(s): 2
- Vendor ID: GenuineIntel
- CPU family: 6
- Model: 106
- Model name: Intel(R) Xeon(R) Silver 4310T CPU @ 2.30GHz
- Stepping: 6
- CPU MHz: 2904.095
- BogoMIPS: 4600.00
- Virtualization: VT-x
- L1d cache: 48K
- L1i cache: 32K
- L2 cache: 1280K
- L3 cache: 15360K
- NUMA node0 CPU(s): 0,2,4,6,8,10,12,14,16,18,20,22,24,26,28,30,32,34,36,38
- NUMA node1 CPU(s): 1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31,33,35,37,39
- Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtrunc pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 invpcid_single intel_pni ssbd mba ibrs i督办 ibpb ibrs_enhanced fs.gsbase tsc_adjust bmi1 hle avx2 smep bmi2 ertz invvpclmulqdq cmqm rdt_as avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha_hni avx512bw avx512vl xsaveopt xsaveopt xsaves xsaveopt xgetbv1 xsaves cmqm_occcll cmqm_mbms_total cmqm_mbms_local split_lock_detect wbnoinvd dtherm ida arat pln pts avx512vmbi umip pku ospke avx512_vmbi gfni vaes vpclmulqdq avx512_vnni avx512_bitalg tme avx512_vpoctndq la57 rdpid md_clear pconfig flush_lld arch_capabilities

(Continued on next page)
Dell Inc.

PowerEdge R750 (Intel Xeon Silver 4310T, 2.30 GHz)

SPEC CPU®2017 Floating Point Rate Result

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CPU2017 License: 55
Test Date: Jun-2021
Test Sponsor: Dell Inc.
Hardware Availability: May-2021
Tested by: Dell Inc.
Software Availability: Feb-2021

Platform Notes (Continued)

/proc/cpuinfo cache data
  cache size : 15360 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
  available: 2 nodes (0-1)
  node 0 cpus: 0 2 4 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34 36 38
  node 0 size: 250968 MB
  node 0 free: 241272 MB
  node 1 cpus: 1 3 5 7 9 11 13 15 17 19 21 23 25 27 29 31 33 35 37 39
  node 1 size: 251034 MB
  node 1 free: 256663 MB
  node distances:
    node  0   1
    0:  10  20
    1:  20  10

From /proc/meminfo
  MemTotal:       527813836 kB
  HugePages_Total:       0
  Hugepagesize:       2048 kB

/sbin/tuned-adm active
  Current active profile: throughput-performance

From /etc/*release* /etc/*version*
  os-release:
    NAME="Red Hat Enterprise Linux"
    VERSION="8.3 (Ootpa)"
    ID="rhel"
    ID_LIKE="fedora"
    VERSION_ID="8.3"
    PLATFORM_ID="platform:el8"
    PRETTY_NAME="Red Hat Enterprise Linux 8.3 (Ootpa)"
    ANSI_COLOR="0;31"
  redhat-release: Red Hat Enterprise Linux release 8.3 (Ootpa)
  system-release: Red Hat Enterprise Linux release 8.3 (Ootpa)
  system-release-cpe: cpe:/o:redhat:enterprise_linux:8.3:ga

uname -a:
  Linux localhost.localdomain 4.18.0-240.15.1.el8_3.x86_64 #1 SMP Wed Feb 3 03:12:15 EST
  2021 x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
  CVE-2018-12207 (iTLB Multihit): Not affected
  CVE-2018-3620 (L1 Terminal Fault): Not affected

(Continued on next page)
**SPEC CPU®2017 Floating Point Rate Result**

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### Platform Notes (Continued)

- **Microarchitectural Data Sampling:** Not affected
- **CVE-2017-5754 (Meltdown):** Not affected
- **CVE-2018-3639 (Speculative Store Bypass):** Mitigation: Speculative Store Bypass disabled via prctl and seccomp
- **CVE-2017-5753 (Spectre variant 1):** Mitigation: usercopy/swapgs barriers and __user pointer sanitization
- **CVE-2017-5715 (Spectre variant 2):** Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
- **CVE-2020-0543 (Special Register Buffer Data Sampling):** Not affected
- **CVE-2019-11135 (TSX Asynchronous Abort):** Not affected

**SPEC is set to:** /mnt/ramdisk2/cpu2017-1.1.5-ic2021.1

<table>
<thead>
<tr>
<th>Filesystem</th>
<th>Type</th>
<th>Size</th>
<th>Used</th>
<th>Avail</th>
<th>Use%</th>
<th>Mounted on</th>
</tr>
</thead>
<tbody>
<tr>
<td>tmpfs</td>
<td>tmpfs</td>
<td>225G</td>
<td>6.9G</td>
<td>219G</td>
<td>4%</td>
<td>/mnt/ramdisk2</td>
</tr>
</tbody>
</table>

From /sys/devices/virtual/dmi/id

- **Vendor:** Dell Inc.
- **Product:** PowerEdge R750
- **Product Family:** PowerEdge
- **Serial:** 1234567

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

- **Memory:**
  - 12x 002C069D002C 18ASF4G72P2Z-3G2E1 32 GB 2 rank 3200, configured at 2666
  - 4x 00AD063200AD HMAA4GR7AJR8N-XN 32 GB 2 rank 3200, configured at 2666
  - 16x Not Specified Not Specified

- **BIOS:**
  - BIOS Vendor: Dell Inc.
  - BIOS Version: 1.2.1
  - BIOS Date: 05/06/2021
  - BIOS Revision: 1.2

(End of data from sysinfo program)

### Compiler Version Notes

| C | 519.lbm_r(base, peak) 538.imagick_r(base, peak) 544.nab_r(base, peak) |

(Continued on next page)
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PowerEdge R750 (Intel Xeon Silver 4310T, 2.30 GHz)

SPEC CPU®2017 Floating Point Rate Result

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Compiler Version Notes (Continued)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
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==============================================================================
C++ | 508.namd_r(base, peak) 510.parest_r(base, peak)
==============================================================================
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================
C++, C | 511.povray_r(peak)
==============================================================================
Intel(R) C++ Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================
C++, C | 511.povray_r(base) 526.blender_r(base, peak)
==============================================================================
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
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==============================================================================
C++, C | 511.povray_r(peak)
==============================================================================
Intel(R) C++ Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
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(Continued on next page)
Compiler Version Notes (Continued)

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C++, C | 511.povray_r(base) 526.blender_r(base, peak)
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C++, C, Fortran | 507.cactuBSSN_r(base, peak)
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Intel(R) 64, Version 2021.1 Build 20201112_000000
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==============================================================================
Fortran | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
         | 554.roms_r(base, peak)
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Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
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==============================================================================
Fortran, C | 521.wrf_r(base, peak) 527.cam4_r(base, peak)
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Intel(R) 64, Version 2021.1 Build 20201112_000000
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Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
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CPU2017 License: 55
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Hardware Availability: May-2021
Software Availability: Feb-2021

Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icx

Benchmarks using both C and C++:
icpx icx

Benchmarks using Fortran, C, and C++:
icpx icx ifort

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.ibm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

(Continued on next page)
Base Optimization Flags (Continued)

C++ benchmarks:
-\texttt{-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -flto}
-\texttt{-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4}
-\texttt{-mbranches-within-32B-boundaries -ljemalloc}
-\texttt{-L/usr/local/jemalloc64-5.0.1/lib}

Fortran benchmarks:
-\texttt{-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div}
-\texttt{-qopt-prefetch -ffinite-math-only}
-\texttt{-qopt-multiple-gather-scatter-by-shuffles -qopt-mem-layout-trans=4}
-\texttt{-nostandard-realloc-lhs -align array32byte -auto}
-\texttt{-mbranches-within-32B-boundaries -ljemalloc}
-\texttt{-L/usr/local/jemalloc64-5.0.1/lib}

Benchmarks using both Fortran and C:
-\texttt{-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math}
-\texttt{-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo}
-\texttt{-no-prec-div -qopt-prefetch -ffinite-math-only}
-\texttt{-qopt-multiple-gather-scatter-by-shuffles}
-\texttt{-mbranches-within-32B-boundaries -nostandard-realloc-lhs}
-\texttt{-align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib}

Benchmarks using both C and C++:
-\texttt{-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math}
-\texttt{-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4}
-\texttt{-mbranches-within-32B-boundaries -ljemalloc}
-\texttt{-L/usr/local/jemalloc64-5.0.1/lib}

Benchmarks using Fortran, C, and C++:
-\texttt{-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math}
-\texttt{-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3}
-\texttt{-no-prec-div -qopt-prefetch -ffinite-math-only}
-\texttt{-qopt-multiple-gather-scatter-by-shuffles}
-\texttt{-mbranches-within-32B-boundaries -nostandard-realloc-lhs}
-\texttt{-align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib}

Peak Compiler Invocation

C benchmarks:
\texttt{icx}

C++ benchmarks:
\texttt{icpx}
**Dell Inc.**

PowerEdge R750 (Intel Xeon Silver 4310T, 2.30 GHz)

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<tr>
<th>SPECrate\textsuperscript{®}2017_fp_base = 170</th>
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<td>SPECrate\textsuperscript{®}2017_fp_peak = 175</td>
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**Peak Compiler Invocation (Continued)**

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icx

Benchmarks using both C and C++:
511.povray\_r: icpc icc
526.blender\_r: icpx icx

Benchmarks using Fortran, C, and C++:
icpx icx ifort

---

**Peak Portability Flags**

Same as Base Portability Flags

---

**Peak Optimization Flags**

C benchmarks:
519.lbm\_r: basepeak = yes
538.imagick\_r: basepeak = yes
544.nab\_r: -w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -flto
-Ofast -qopt-mem-layout-trans=4
-fimf-accuracy-bits=14:sqrt
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

C++ benchmarks:
508.namd\_r: basepeak = yes
510.parest\_r: -w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

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**SPEC CPU®2017 Floating Point Rate Result**

**Dell Inc.**

**PowerEdge R750 (Intel Xeon Silver 4310T, 2.30 GHz)**

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**Software Availability:** Feb-2021

---

**Peak Optimization Flags (Continued)**

Fortran benchmarks:

- `503.bwaves_r: basepeak = yes`
- `549.fotonik3d_r: basepeak = yes`

Benchmarks using both Fortran and C:

- `521.wrf_r: basepeak = yes`
- `527.cam4_r: basepeak = yes`

Benchmarks using both C and C++:


- `526.blender_r: basepeak = yes`

Benchmarks using Fortran, C, and C++:

- `507.cactuBSSN_r: basepeak = yes`

---

The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:

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