Hewlett Packard Enterprise
(Test Sponsor: HPE)
ProLiant DL360 Gen10 Plus
(2.30 GHz, Intel Xeon Silver 4316)

SPECrates

SPECrates\textsuperscript{2017 fp base} = 293
SPECrates\textsuperscript{2017 fp peak} = 305

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Hardware

CPU Name: Intel Xeon Silver 4316
Max MHz: 3400
Nominal: 2300
Enabled: 40 cores, 2 chips, 2 threads/core
Orderable: 1, 2 chip(s)
Cache L1: 32 KB I + 48 KB D on chip per core
L2: 1.25 MB I+D on chip per core
L3: 30 MB I+D on chip per chip
Other: None
Memory: 2 TB (32 x 64 GB 2Rx4 PC4-3200AA-R, running at 2666)
Storage: 1 x 400 GB SAS SSD, RAID 0
Other: None

Software

OS: Red Hat Enterprise Linux 8.3 (Ootpa)
Kernel 4.18.0-240.el8.x86_64
Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++
Compiler Build 20201113 for Linux;
Fortran: Version 2021.1 of Intel Fortran Compiler
Classic Build 20201112 for Linux;
C/C++: Version 2021.1 of Intel C/C++ Compiler
Classic Build 20201112 for Linux
Parallel: No
Firmware: HPE BIOS Version U46 v1.42 05/16/2021 released May-2021
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: jemalloc memory allocator V5.0.1

(Continued on next page)
SPEC CPU® 2017 Floating Point Rate Result

Hewlett Packard Enterprise
(Test Sponsor: HPE)
ProLiant DL360 Gen10 Plus
(2.30 GHz, Intel Xeon Silver 4316)

SPECrate® 2017_fp_base = 293
SPECrate® 2017_fp_peak = 305

Results Table

<table>
<thead>
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<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
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<td>430</td>
<td>148</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3 > /proc/sys/vm/drop_caches

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = 
"/home/cpu2017_1.1.8/lib/intel64:/home/cpu2017_1.1.8/je5.0.1-64"
MALLOCONF = "retain:true"
General Notes

Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM
memory using Red Hat Enterprise Linux 8.1
runcpu command invoked through numacll i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Submitted by: "Bhatnagar, Prateek" <prateek.bhatnagar@hpe.com>
Submitted: Mon Jun 21 10:35:38 EDT 2021
Submission: cpu2017-20210621-27602.sub

Platform Notes

The system ROM used for this result contains Intel microcode version 0xd0002a0 for
the Intel Xeon Silver 4316 processor.

BIOS Configuration:
Workload Profile set to General Throughput Compute
Memory Patrol Scrubbing set to Disabled
Advanced Memory Protection set to Advanced ECC
Last Level Cache (LLC) Prefetch set to Enabled
Last Level Cache (LLC) Dead Line Allocation set to Disabled
Enhanced Processor Performance set to Enabled
Enhanced Processor Performance Profile set to Aggressive
Thermal Configuration set to Maximum Cooling
Workload Profile set to Custom
DCU Stream Prefetcher set to Disabled
XPT Remote Prefetcher set to Enabled
Energy/Performance Bias set to Balanced Performance

Sysinfo program /home/cpu2017_1.1.8/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acac64d
running on localhost.localdomain Thu Jun 17 23:49:14 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4316 CPU @ 2.30GHz

(Continued on next page)
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SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

SPECrate®2017_fp_base = 293
SPECrate®2017_fp_peak = 305

Platform Notes (Continued)

2 "physical id"s (chips)
80 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 20
siblings : 40
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19

From lscpu from util-linux 2.32.1:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 80
On-line CPU(s) list: 0-79
Thread(s) per core: 2
Core(s) per socket: 20
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Silver 4316 CPU @ 2.30GHz
Stepping: 6
CPU MHz: 824.076
BogoMIPS: 4600.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 30720K
NUMA node0 CPU(s): 0-9,40-49
NUMA node1 CPU(s): 10-19,50-59
NUMA node2 CPU(s): 20-29,60-69
NUMA node3 CPU(s): 30-39,70-79
Flags: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmpref pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtr pdcm pdcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invpcid_single ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vmmi flexpriority ept vpid ept_ad fsbegbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid cqm aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invpcid_single ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vmmi flexpriority ept vpid ept_ad fsbegbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid cqm aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invpcid_single ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vmmi flexpriority ept vpid ept_ad fsbegbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid cqm aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invpcid_single ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vmmi flexpriority ept vpid ept_ad fsbegbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid cqm aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invpcid_single ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vmmi flexpriority ept vpid ept_ad fsbegbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid cqm aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invpcid_single ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vmmi flexpriority ept vpid ept_ad fsbegbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid cqm aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invpcid_single ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vmmi flexpriority ept vpid ept_ad fsbegbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid cqm aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invpcid_single ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vmmi flexpriority ept vpid ept_ad fsbegbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid cqm aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invpcid_single ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vmmi flexpriority ept vpid ept_ad fsbegbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid cqm aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invpcid_single ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vmmi flexpriority ept vpid ept_ad fsbegbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid cqm aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invpcid_single ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vmmi flexpriority ept vpid ept_ad fsbegbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid cqm aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invpcid_single ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vmmi flexpriority ept vpid ept_ad fsbegbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid cqm aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid Fault epb cat_13 invpcid Single ssbd mba ibrs ibpb stibp ibrs enhanced tpr_shadow vmmi flexpriority ept vpid ept_ad fsbegbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha ni avx512bw avx512vl xsaveopt xsaves xgetbv v cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local split lock detect wbnoinvd dtherm ida arat pin pts avx512vbmi umip pku ospke avx512_vbmi2 gfni vaes vpcm logdq avx512_vnni avx512_bitalg tme

(Continued on next page)
SPEC CPU®2017 Floating Point Rate Result

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SPECrate®2017_fp_base = 293
SPECrate®2017_fp_peak = 305

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Platform Notes (Continued)

avx512_vpopcntdq la57 rdpid md_clear pconfig flush_l1d arch_capabilities

/proc/cpuinfo cache data
    cache size : 30720 KB

From numactl --hardware
WARNING: a numactl 'node' might or might not correspond to a physical chip.
    available: 4 nodes (0-3)
    node 0 cpus: 0 1 2 3 4 5 6 7 8 9 40 41 42 43 44 45 46 47 48 49
    node 0 size: 506169 MB
    node 0 free: 515328 MB
    node 1 cpus: 10 11 12 13 14 15 16 17 18 19 50 51 52 53 54 55 56 57 58 59
    node 1 size: 506414 MB
    node 1 free: 515612 MB
    node 2 cpus: 20 21 22 23 24 25 26 27 28 29 60 61 62 63 64 65 66 67 68 69
    node 2 size: 506774 MB
    node 2 free: 515797 MB
    node 3 cpus: 30 31 32 33 34 35 36 37 38 39 70 71 72 73 74 75 76 77 78 79
    node 3 size: 506186 MB
    node 3 free: 515786 MB
    node distances:
        node 0 1 2 3
        0: 10 20 30 30
        1: 20 10 30 30
        2: 30 30 10 20
        3: 30 30 20 10

From /proc/meminfo
    MemTotal: 2113484736 kB
    HugePages_Total: 0
    Hugepagesize: 2048 kB

/sbin/tuned-adm active
    Current active profile: throughput-performance

From /etc/*release* /etc/*version*
    os-release:
        NAME="Red Hat Enterprise Linux"
        VERSION="8.3 (Ootpa)"
        ID="rhel"
        ID_LIKE="fedora"
        VERSION_ID="8.3"
        PLATFORM_ID="platform:el8"
        PRETTY_NAME="Red Hat Enterprise Linux 8.3 (Ootpa)"
        ANSI_COLOR="0;31"
        redhat-release: Red Hat Enterprise Linux release 8.3 (Ootpa)
        system-release: Red Hat Enterprise Linux release 8.3 (Ootpa)

(Continued on next page)
Hewlett Packard Enterprise
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SPECrate®2017_fp_base = 293
SPECrate®2017_fp_peak = 305

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Test Date: Jun-2021
Hardware Availability: Jun-2021
Software Availability: Jun-2021

Platform Notes (Continued)

system-release-cpe: cpe:/o:redhat:enterprise_linux:8.3:ga

uname -a:
Linux localhost.localdomain 4.18.0-240.el8.x86_64 #1 SMP Wed Sep 23 05:13:10 EDT 2020
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass):
Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1):
Mitigation: usercopy/swapgs barriers and __user_pointer sanitization
CVE-2017-5715 (Spectre variant 2):
Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Jun 17 23:48

SPEC is set to: /home/cpu2017_1.1.8

Filesystem              Type  Size  Used Avail Use% Mounted on
/dev/mapper/rhel00-home xfs   372G  219G  153G  59% /home

From /sys/devices/virtual/dmi/id
Vendor: HPE
Product: ProLiant DL360 Gen10 Plus
Product Family: ProLiant
Serial: CN701108CQ

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
32x Micron 36ASF8G72PZ-3G2B2 64 GB 2 rank 3200, configured at 2666

BIOS:
BIOS Vendor: HPE
BIOS Version: U46
BIOS Date: 05/16/2021
BIOS Revision: 1.42

(Continued on next page)
Platform Notes (Continued)

Firmware Revision: 2.42

(End of data from sysinfo program)

Compiler Version Notes

========================================================================================================
C               | 519.lbm_r(base, peak) 538.imagick_r(base, peak)
| 544.nab_r(base, peak)
========================================================================================================
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

========================================================================================================
C++             | 508.namd_r(base, peak) 510.parest_r(base, peak)
========================================================================================================
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

========================================================================================================
C++, C          | 511.povray_r(peak)
========================================================================================================
Intel(R) C++ Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

========================================================================================================
C++, C          | 511.povray_r(base) 526.blender_r(base, peak)
========================================================================================================
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
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(Continued on next page)
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ProLiant DL360 Gen10 Plus
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SPECrate®2017_fp_base = 293
SPECrate®2017_fp_peak = 305

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

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Compiler Version Notes (Continued)

C++, C          | 511.povray_r(peak)

Intel(R) C++ Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

C++, C          | 511.povray_r(base) 526.blender_r(base, peak)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

C++, C, Fortran | 507.cactuBSSN_r(base, peak)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64, Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Fortran         | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
554.roms_r(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Fortran, C      | 521.wrf_r(base, peak) 527.cam4_r(base, peak)

(Continued on next page)
Hewlett Packard Enterprise
(Test Sponsor: HPE)
ProLiant DL360 Gen10 Plus
(2.30 GHz, Intel Xeon Silver 4316)

SPECrater®2017_fp_base = 293
SPECrater®2017_fp_peak = 305

Compiler Version Notes (Continued)

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icx

Benchmarks using both C and C++:
icpx icx

Benchmarks using Fortran, C, and C++:
icpx icx ifort

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.ibm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64
Hewlett Packard Enterprise
(Test Sponsor: HPE)
ProLiant DL360 Gen10 Plus
(2.30 GHz, Intel Xeon Silver 4316)

SPECrate®2017_fp_base = 293
SPECrate®2017_fp_peak = 305

CPU2017 License: 3
Test Sponsor: HPE
Test Date: Jun-2021
Hardware Availability: Jun-2021
Tested by: HPE
Software Availability: Jun-2021

Base Optimization Flags

C benchmarks:
-\texttt{-w -std=\texttt{c11} -m64 -Wl,\texttt{-z},muldefs -xCORE-AVX512 -Ofast -ffast-math}
-\texttt{-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4}
-\texttt{-mbranches-within-32B-boundaries -ljemalloc}
-\texttt{-L/usr/local/jemalloc64-5.0.1/lib}

C++ benchmarks:
-\texttt{-w -m64 -Wl,\texttt{-z},muldefs -xCORE-AVX512 -Ofast -ffast-math -flto}
-\texttt{-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4}
-\texttt{-mbranches-within-32B-boundaries -ljemalloc}
-\texttt{-L/usr/local/jemalloc64-5.0.1/lib}

Fortran benchmarks:
-\texttt{-w -m64 -Wl,\texttt{-z},muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div}
-\texttt{-qopt-prefetch -ffinite-math-only}
-\texttt{-qopt-multiple-gather-scatter-by-shuffles -qopt-mem-layout-trans=4}
-\texttt{-nostandard-realloc-lhs -align array32byte -auto}
-\texttt{-mbranches-within-32B-boundaries -ljemalloc}
-\texttt{-L/usr/local/jemalloc64-5.0.1/lib}

Benchmarks using both Fortran and C:
-\texttt{-w -m64 -std=\texttt{c11} -Wl,\texttt{-z},muldefs -xCORE-AVX512 -Ofast -ffast-math}
-\texttt{-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo}
-\texttt{-no-prec-div -qopt-prefetch -ffinite-math-only}
-\texttt{-qopt-multiple-gather-scatter-by-shuffles}
-\texttt{-mbranches-within-32B-boundaries -nostandard-realloc-lhs}
-\texttt{-align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib}

Benchmarks using both C and C++:
-\texttt{-w -m64 -std=\texttt{c11} -Wl,\texttt{-z},muldefs -xCORE-AVX512 -Ofast -ffast-math}
-\texttt{-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4}
-\texttt{-mbranches-within-32B-boundaries -ljemalloc}
-\texttt{-L/usr/local/jemalloc64-5.0.1/lib}

Benchmarks using Fortran, C, and C++:
-\texttt{-w -m64 -std=\texttt{c11} -Wl,\texttt{-z},muldefs -xCORE-AVX512 -Ofast -ffast-math}
-\texttt{-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3}
-\texttt{-no-prec-div -qopt-prefetch -ffinite-math-only}
-\texttt{-qopt-multiple-gather-scatter-by-shuffles}
-\texttt{-mbranches-within-32B-boundaries -nostandard-realloc-lhs}
-\texttt{-align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib}
## Peak Compiler Invocation

C benchmarks:
- icx

C++ benchmarks:
- icpx

Fortran benchmarks:
- ifort

Benchmarks using both Fortran and C:
- ifort icx

Benchmarks using both C and C++:
- 511.povray_r: icpc icc
- 526.blender_r: icpx icx

Benchmarks using Fortran, C, and C++:
- icpx icx ifort

## Peak Portability Flags

Same as Base Portability Flags

## Peak Optimization Flags

C benchmarks:
- 519.lbm_r: basepeak = yes
- 538.imagick_r: basepeak = yes
- 544.nab_r: -w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -flto
  -Ofast -qopt-mem-layout-trans=4
  -fimf-accuracy-bits=14:sqrt
  -mbranches-within-32B-boundaries -ljemalloc
  -L/usr/local/jemalloc64-5.0.1/lib

C++ benchmarks:

(Continued on next page)
Peak Optimization Flags (Continued)

508.namd_r: basepeak = yes

510.parest_r: -w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
   -flto -mfpmath=sse -funroll-loops
   -qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
   -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

Fortran benchmarks:

503.bwaves_r: basepeak = yes

549.fotonik3d_r: basepeak = yes

554.roms_r: -w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo
   -no-prec-div -qopt-prefetch -ffinite-math-only
   -qopt-multiple-gather-scatter-by-shuffles
   -qopt-mem-layout-trans=4 -nostandard-realloc-lhs
   -align array32byte -auto -mbranches-within-32B-boundaries
   -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using both Fortran and C:

521.wrf_r: basepeak = yes

527.cam4_r: basepeak = yes

Benchmarks using both C and C++:

511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3
   -ipo -no-prec-div -qopt-prefetch -ffinite-math-only
   -qopt-multiple-gather-scatter-by-shuffles
   -qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
   -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

526.blender_r: basepeak = yes

Benchmarks using Fortran, C, and C++:

507.cactuBSSN_r: basepeak = yes

The flags files that were used to format this result can be browsed at

http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.0-ICX-revC.html
## SPEC CPU®2017 Floating Point Rate Result

### Hewlett Packard Enterprise
- **(Test Sponsor: HPE)**
- **ProLiant DL360 Gen10 Plus**
- **(2.30 GHz, Intel Xeon Silver 4316)**

<table>
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<tr>
<th>SPECrate®2017_fp_base</th>
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</tr>
</thead>
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<td>293</td>
<td>305</td>
</tr>
</tbody>
</table>

### Tested by:
- **HPE**

### Test Sponsor:
- **HPE**

### Hardware Availability:
- **Jun-2021**

### Software Availability:
- **Jun-2021**

### CPU2017 License:
- **3**

### Test Date:
- **Jun-2021**

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You can also download the XML flags sources by saving the following links:

- [http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.0-ICX-revC.xml](http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.0-ICX-revC.xml)

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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