# Lenovo Global Technology

**ThinkSystem SR650 V2**

(2.20 GHz, Intel Xeon Platinum 8352S)

<table>
<thead>
<tr>
<th>Hardware</th>
<th>Software</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Name: Intel Xeon Platinum 8352S</td>
<td>OS: SUSE Linux Enterprise Server 15 SP2 (x86_64)</td>
</tr>
<tr>
<td>Max MHz: 3400</td>
<td>Kernel 5.3.18-22-default</td>
</tr>
<tr>
<td>Nominal: 2200</td>
<td>Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++</td>
</tr>
<tr>
<td>Enabled: 64 cores, 2 chips</td>
<td>Compiler Build 20201113 for Linux;</td>
</tr>
<tr>
<td>Orderable: 1,2 chips</td>
<td>Fortran: Version 2021.1 of Intel Fortran Compiler</td>
</tr>
<tr>
<td>Cache L1: 32 KB I + 48 KB D on chip per core</td>
<td>Classic Build 20201112 for Linux;</td>
</tr>
<tr>
<td>L2: 1.25 MB I+D on chip per core</td>
<td>C/C++: Version 2021.1 of Intel C/C++ Compiler</td>
</tr>
<tr>
<td>L3: 48 MB I+D on chip per chip</td>
<td>Classic Build 20201112 for Linux</td>
</tr>
<tr>
<td>Other: None</td>
<td>Parallel: No</td>
</tr>
<tr>
<td>Memory: 1 TB (32 x 32 GB 2Rx8 PC4-3200AA-R)</td>
<td>Firmware: Lenovo BIOS Version AFE109PT1 1.00</td>
</tr>
<tr>
<td>Storage: 1 x 960 GB SATA SSD</td>
<td>released Apr-2021</td>
</tr>
<tr>
<td>Other: None</td>
<td>File System: xfs</td>
</tr>
</tbody>
</table>

## SPEC CPU®2017 Floating Point Rate Result

**Lenovo Global Technology**

**ThinkSystem SR650 V2**

(2.20 GHz, Intel Xeon Platinum 8352S)

**SPECrade®2017_fp_base = 398**

**SPECrade®2017_fp_peak = Not Run**

**Lenovo Global Technology**

**Test Sponsor:** Lenovo Global Technology

**Test Date:** May-2021

**Hardware Availability:** Jul-2021

**Test Date:** May-2021

**Software Availability:** Feb-2021

**Tested by:** Lenovo Global Technology

**CPU2017 License:** 9017

<table>
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</tr>
<tr>
<td>64</td>
<td>375</td>
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<tr>
<td>64</td>
<td>403</td>
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<tr>
<td>64</td>
<td>1090</td>
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<tr>
<td>64</td>
<td>578</td>
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<tr>
<td>64</td>
<td>228</td>
</tr>
<tr>
<td>64</td>
<td>193</td>
</tr>
</tbody>
</table>

**SPECrate®2017_fp_base (398)**

**CPU Name:** Intel Xeon Platinum 8352S

**Max MHz:** 3400

**Nominal:** 2200

**Enabled:** 64 cores, 2 chips

**Orderable:** 1,2 chips

**Cache L1:** 32 KB I + 48 KB D on chip per core

**L2:** 1.25 MB I+D on chip per core

**L3:** 48 MB I+D on chip per chip

**Other:** None

**Memory:** 1 TB (32 x 32 GB 2Rx8 PC4-3200AA-R)

**Storage:** 1 x 960 GB SATA SSD

**Other:** None

**Hardware Availability:** Jul-2021

**Software Availability:** Feb-2021

**Tested by:** Lenovo Global Technology

**CPU2017 License:** 9017

**Test Sponsor:** Lenovo Global Technology

**Test Date:** May-2021

**Software Availability:** Feb-2021

**Tested by:** Lenovo Global Technology

**CPU2017 License:** 9017
## Lenovo Global Technology

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(2.20 GHz, Intel Xeon Platinum 8352S)

**CPU2017 License:** 9017  
**Test Sponsor:** Lenovo Global Technology  
**Tested by:** Lenovo Global Technology

**Test Date:** May-2021  
**Hardware Availability:** Jul-2021  
**Software Availability:** Feb-2021

---

### Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Base Seconds</th>
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<th>Base Seconds</th>
<th>Base Ratio</th>
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<td>554.roms_r</td>
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<td>528</td>
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<td>193</td>
</tr>
</tbody>
</table>

**SPECrate**

**SPECrate2017_fp_base =** 398  
**SPECrate2017_fp_peak =** Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

---

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

---

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

---

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:

```bash
LD_LIBRARY_PATH = 
"/home/cpu2017-1.1.5-ic2021.1-revA-update1/lib/intel64:/home/cpu2017-1.1 .5-ic2021.1-revA-update1/je5.0.1-64"  
MALLOCC_CONF = "retain:true"
```

---

### General Notes

Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM  
memory using openSUSE Leap 15.2  
Transparent Huge Pages enabled by default

(Continued on next page)
### Lenovo Global Technology

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**SPECration®2017_fp_base = 398**  
**SPECration®2017_fp_peak = Not Run**

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9017</th>
<th>Test Date:</th>
<th>May-2021</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Lenovo Global Technology</td>
<td>Hardware Availability:</td>
<td>Jul-2021</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Lenovo Global Technology</td>
<td>Software Availability:</td>
<td>Feb-2021</td>
</tr>
</tbody>
</table>

#### General Notes (Continued)

Prior to runcpu invocation
Filesystem page cache synced and cleared with:
`sync; echo 3 > /proc/sys/vm/drop_caches`

runcpu command invoked through numactl i.e.:
`numactl --interleave=all runcpu <etc>`

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation  
built with the Redhat Enterprise 7.5, and the system compiler gcc 4.8.5  

#### Platform Notes

**BIOS configuration:**
Choose Operating Mode set to Maximum Performance  
Hyper-Threading set to Disabled  
DCU Streamer Prefetcher set to Disabled  
DCU IP Prefetcher set to Disabled  
SNC set to Enabled  
Patrol Scrub set to Disabled

**Sysinfo program**  
/home/cpu2017-1.1.5-ic2021.1-revA-update1/bin/sysinfo
Rev: r6538 of 2020-09-24 e8664e66d2d7080afea89d4b38e2f1c  
running on localhost Sat May 15 07:16:06 2021

**SUT (System Under Test) info as seen by some common utilities.**
For more information on this section, see  
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From `/proc/cpuinfo`

```
model name : Intel(R) Xeon(R) Platinum 8352S CPU @ 2.20GHz
  2 "physical id"s (chips)
  64 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 32
siblings : 32
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
```

(Continued on next page)
Platform Notes (Continued)

From lscpu:

Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 57 bits virtual
CPU(s): 64
On-line CPU(s) list: 0-63
Thread(s) per core: 1
Core(s) per socket: 32
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 106
Model name: Intel(R) Xeon(R) Platinum 8352S CPU @ 2.20GHz
Stepping: 6
CPU MHz: 2800.020
BogoMIPS: 4400.00
Virtualization: VT-x
L1d cache: 48K
L1i cache: 32K
L2 cache: 1280K
L3 cache: 49152K
NUMA node0 CPU(s): 0-15
NUMA node1 CPU(s): 16-31
NUMA node2 CPU(s): 32-47
NUMA node3 CPU(s): 48-63
Flags: fpu vme de pse tsc msr pae mce cmx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmerf pni pclmulqdq dtes64 ms_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm
pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c
rdram lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 invpcid_single ssbd mba ibrs
ibpb stibp ibrs_enhanced tpr_shadow vmmx flexpriority ept vpid ept_ad fsgssbase
tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm rdt_a avx512f avx512dq
dseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha ni avx512bw
avx512vl xsaveopt xsavec xsavec xsaveProperties cqm_llc cqm_occupa llc cqm_mbb_total
cqm_mbb_local wbinvd dtcpcn ida arat plot psl pts avx512vmbmi umip kpu ospke
avx512_vbmi2 gfni vaes vpclmulqdq avx512_vnni avx512_bitalg tme avx512_vpopcntdq
la57 rdrpid md_clear pconfig flush_lld arch_capabilities

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 4 nodes (0-3)

(Continued on next page)
## Lenovo Global Technology

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(2.20 GHz, Intel Xeon Platinum 8352S)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base</th>
<th>SPECrate®2017_fp_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>398</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

### Platform Notes (Continued)

- **node 0 cpus:** 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
- **node 0 size:** 257634 MB
- **node 0 free:** 257297 MB
- **node 1 cpus:** 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
- **node 1 size:** 258043 MB
- **node 1 free:** 257640 MB
- **node 2 cpus:** 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47
- **node 2 size:** 258043 MB
- **node 2 free:** 257828 MB
- **node 3 cpus:** 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63
- **node 3 size:** 258007 MB
- **node 3 free:** 257771 MB
- **node distances:**
  - 0: 10 11 20 20
  - 1: 11 10 20 20
  - 2: 20 20 10 11
  - 3: 20 20 11 10

From `/proc/meminfo`

- **MemTotal:** 1056491216 kB
- **HugePages_Total:** 0
- **Hugepagesize:** 2048 kB

```
/usr/bin/lsb_release -d
SUSE Linux Enterprise Server 15 SP2
```

```
From /etc/*release* /etc/*version*

os-release:
- NAME="SLES"
- VERSION="15-SP2"
- VERSION_ID="15.2"
- PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
- ID="sles"
- ID_LIKE="suse"
- ANSI_COLOR="0;32"
- CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
- Linux localhost 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

- CVE-2018-12207 (iTLB Multihit): Not affected
- CVE-2018-3620 (L1 Terminal Fault): Not affected
- Microarchitectural Data Sampling: Not affected

(Continued on next page)
Platform Notes (Continued)

CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapsgs barriers and __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 May 15 02:20

SPEC is set to: /home/cpu2017-1.1.5-ic2021.1-revA-update1
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda3 xfs 891G 23G 868G 3% /

From /sys/devices/virtual/dmi/id
Vendor: Lenovo
Product: ThinkSystem SR650 V2 MB
Product Family: ThinkSystem
Serial: 1234567890

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
32x Samsung M393A4G43AB3-CWE 32 GB 2 rank 3200

BIOS:
  BIOS Vendor: Lenovo
  BIOS Version: AFE109PT1-1.00
  BIOS Date: 04/28/2021
  BIOS Revision: 1.0
  Firmware Revision: 1.0

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
<table>
<thead>
<tr>
<th>C</th>
<th>519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)</th>
</tr>
</thead>
</table>

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Lenovo Global Technology
ThinkSystem SR650 V2
(2.20 GHz, Intel Xeon Platinum 8352S)

SPECrate®2017_fp_base = 398
SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9017
Test Sponsor: Lenovo Global Technology
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Test Date: May-2021
Hardware Availability: Jul-2021
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Compiler Version Notes (Continued)

---

C++             | 508.namd_r(base) 510.parest_r(base)
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
---

C++, C          | 511.povray_r(base) 526.blender_r(base)
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
---

C++, C, Fortran | 507.cactuBSSN_r(base)
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
---

Fortran          | 503.bwaves_r(base) 549.fotonik3d_r(base) 554.roms_r(base)
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
---

Fortran, C      | 521.wrf_r(base) 527.cam4_r(base)

(Continued on next page)
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Compiler Version Notes (Continued)

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icx
C++ benchmarks:
icpx
Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icx

Benchmarks using both C and C++:
icpx icx

Benchmarks using Fortran, C, and C++:
icpx icx ifort

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.ibm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64

(Continued on next page)
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Base Portability Flags (Continued)

554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

C++ benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Fortran benchmarks:
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
-qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using both Fortran and C:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
-qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using both C and C++:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo
-qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib

Benchmarks using Fortran, C, and C++:
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo
-qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -nostandard-realloc-lhs

(Continued on next page)
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Test Date: May-2021
Hardware Availability: Jul-2021
Software Availability: Feb-2021

Base Optimization Flags (Continued)
Benchmarks using Fortran, C, and C++ (continued):
-align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Lenovo-Platform-SPECcpu2017-Flags-V1.2-ICElake-D.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Lenovo-Platform-SPECcpu2017-Flags-V1.2-ICElake-D.xml
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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