Hewlett Packard Enterprise
(Test Sponsor: HPE)
ProLiant DL380 Gen10 Plus
(3.10 GHz, Intel Xeon Gold 6346)

SPECspeed®2017_int_base = 12.1
SPECspeed®2017_int_peak = 12.4

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<th>SPECspeed®2017_int_peak (12.4)</th>
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<td>602.gcc_s 64</td>
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<td>625.x264_s 64</td>
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<td>641.leela_s 64</td>
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<td>648.exchange2_s 64</td>
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<tr>
<td>657.xz_s 64</td>
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</tbody>
</table>

**Hardware**

- **CPU Name:** Intel Xeon Gold 6346
- **Max MHz:** 3600
- **Nominal:** 3100
- **Enabled:** 32 cores, 2 chips, 2 threads/core
- **Orderable:** 1, 2 chip(s)
- **Cache L1:** 32 KB I + 48 KB D on chip per core
- **L2:** 1.25 MB I+D on chip per core
- **L3:** 36 MB I+D on chip per chip
- **Memory:** 2 TB (32 x 64 GB 2Rx4 PC4-3200AA-R)
- **Storage:** 1 x 800 GB SAS SSD, RAID 0

**Software**

- **OS:** Red Hat Enterprise Linux 8.3 (Ootpa)
- **Compiler:** C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux;
  Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux;
  C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux
- **Parallel:** Yes
- **Firmware:** HPE BIOS Version U46 v1.42 05/16/2021 released Jun-2021
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 64-bit
- **Other:** jemalloc memory allocator V5.0.1
- **Power Management:** BIOS set to prefer performance at the cost of additional power usage
SPEC CPU®2017 Integer Speed Result

Hewlett Packard Enterprise
(Test Sponsor: HPE)
ProLiant DL380 Gen10 Plus
(3.10 GHz, Intel Xeon Gold 6346)

Copyright 2017-2021 Standard Performance Evaluation Corporation

Hewlett Packard Enterprise
(Test Sponsor: HPE)
ProLiant DL380 Gen10 Plus
(3.10 GHz, Intel Xeon Gold 6346)

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

SPECspeed®2017_int_base = 12.1
SPECspeed®2017_int_peak = 12.4

Results Table

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<td>64</td>
<td>260</td>
<td>23.8</td>
<td>260</td>
<td>23.8</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
    sync; echo 3>       /proc/sys/vm/drop_caches

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,scatter"
LD_LIBRARY_PATH = "/home/cpu2017_1.1.8/lib/intel64:/home/cpu2017_1.1.8/je5.0.1-64"
MALLOC_CONF = "retain:true"
OMP_STACKSIZE = "192M"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM
memory using Redhat Enterprise Linux 8.0
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation

(Continued on next page)
Hewlett Packard Enterprise
(Test Sponsor: HPE)
ProLiant DL380 Gen10 Plus
(3.10 GHz, Intel Xeon Gold 6346)

SPECspeed®2017_int_base = 12.1
SPECspeed®2017_int_peak = 12.4

General Notes (Continued)

built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Submitted by: "Bhatnagar, Prateek" <prateek.bhatnagar@hpe.com>
Submitted: Mon May 24 12:53:22 EDT 2021
Submission: cpu2017-20210524-26468.sub

Submitted by: "Bhatnagar, Prateek" <prateek.bhatnagar@hpe.com>
Submitted: Tue Jun  1 09:11:53 EDT 2021
Submission: cpu2017-20210524-26468.sub

Platform Notes

The system ROM used for this result contains Intel microcode version 0xd0002a0
for the Intel Xeon Platinum 6346 processor.
BIOS Configuration:
Workload Profile set to General Peak Frequency Compute
Thermal Configuration set to Maximum Cooling
Memory Patrol Scrubbing set to Disabled
Last Level Cache (LLC) Prefetch set to Enabled
Last Level Cache (LLC) Dead Line Allocation set to Disabled
Advanced Memory Protection set to Advanced ECC
Enhanced Processor Performance set to Enabled
Workload Profile set to Custom
Energy/Performance Bias set to Balanced Power
DCU Stream Prefetcher set to Disabled
Adjacent Sector Prefetch set to Disabled
Minimum Processor Idle Power Package C-State set to No Package State
Numa Group Size Optimization set to Flat

Sysinfo program /home/cpu2017_1.1.8/bin/sysinfo
Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acaf64d
running on localhost.localdomain Fri Jun 22 16:49:09 2018

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
 model name : Intel(R) Xeon(R) Gold 6346 CPU @ 3.10GHz
  2  "physical id"s (chips)
  64 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 16
siblings : 32

(Continued on next page)
**SPEC CPU®2017 Integer Speed Result**

**Hewlett Packard Enterprise**  
**Test Sponsor:** HPE  
**ProLiant DL380 Gen10 Plus**  
**(3.10 GHz, Intel Xeon Gold 6346)**

<table>
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<th>May-2021</th>
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<td>Hardware Availability:</td>
<td>Jun-2021</td>
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<td>Software Availability:</td>
<td>Jun-2021</td>
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</tbody>
</table>

### SPECspeed®2017_int_base = 12.1

### SPECspeed®2017_int_peak = 12.4

**Platform Notes (Continued)**

physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15  
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lscpu from util-linux 2.32.1:
- **Architecture:** x86_64
- **CPU op-mode(s):** 32-bit, 64-bit
- **Byte Order:** Little Endian
- **CPU(s):** 64
- **On-line CPU(s) list:** 0-63
- **Thread(s) per core:** 2
- **Core(s) per socket:** 16
- **Socket(s):** 2
- **NUMA node(s):** 2
- **Vendor ID:** GenuineIntel
- **CPU family:** 6
- **Model:** 106
- **Model name:** Intel(R) Xeon(R) Gold 6346 CPU @ 3.10GHz
- **Stepping:** 6
- **CPU MHz:** 1262.544
- **BogoMIPS:** 6200.00
- **Virtualization:** VT-x
- **L1d cache:** 48K
- **L1i cache:** 32K
- **L2 cache:** 1280K
- **L3 cache:** 36864K
- **NUMA node0 CPU(s):** 0-15,32-47
- **NUMA node1 CPU(s):** 16-31,48-63
- **Flags:** fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 invpcid_single ssbd mba ibrs ibpb ibrs_enhanced tpr_shadow vnmi flexpriority ept vpid ept_ad fssavebase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid cqm rdt_a avx512f avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha_hl avx512bw avx512vl xsavesopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local split_lock_detect wbnoiwvd dtherm ida arat pni pts avx512vbmi ument pku ospke avx512_vbmi2 gfn i vaes vcpulunqdq avx512_vnni avx512_bitalg tme avx512_vpopcntdq la57 rdpid md_clear pconfig flush_l1d arch_capabilities

/proc/cpuinfo cache data
- **cache size:** 36864 KB

From numactl --hardware  
**WARNING:** a numactl 'node' might or might not correspond to a physical chip.  
available: 2 nodes (0-1)

(Continued on next page)
**SPEC CPU®2017 Integer Speed Result**

**Hewlett Packard Enterprise**  
(Test Sponsor: HPE)  
ProLiant DL380 Gen10 Plus  
(3.10 GHz, Intel Xeon Gold 6346)  

<table>
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<tr>
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<tr>
<td>SPECspeed®2017_int_peak</td>
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<td>Software Availability</td>
<td>Jun-2021</td>
</tr>
</tbody>
</table>

### Platform Notes (Continued)

```
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47
node 0 size: 982044 MB
node 0 free: 912554 MB
node 1 cpus: 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63
node 1 size: 977821 MB
node 1 free: 911571 MB
node distances:
node 0 1
0: 10 20
1: 20 10
```

From /proc/meminfo

```
MemTotal:       2113488308 kB
HugePages_Total:       0
Hugepagesize:       2048 kB
```

/sbin/tuned-adm active

```
Current active profile: throughput-performance
```

From /etc/*release* /etc/*version*

```
NAME="Red Hat Enterprise Linux"
VERSION="8.3 (Ootpa)"
ID="rhel"
ID_LIKE="fedora"
VERSION_ID="8.3"
PLATFORM_ID="platform:el8"
PRETTY_NAME="Red Hat Enterprise Linux 8.3 (Ootpa)"
ANSI_COLOR="0;31"
redhat-release: Red Hat Enterprise Linux release 8.3 (Ootpa)
system-release: Red Hat Enterprise Linux release 8.3 (Ootpa)
system-release-cpe: cpe:/o:redhat:enterprise_linux:8.3:ga
```

uname -a:

```
Linux localhost.localdomain 4.18.0-240.el8.x86_64 #1 SMP Wed Sep 23 05:13:10 EDT 2020
x86_64 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

```
CVE-2018-12207 (iTLB Multihit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and
```

(Continued on next page)
SPEC CPU®2017 Integer Speed Result

Hewlett Packard Enterprise
(Test Sponsor: HPE)
ProLiant DL380 Gen10 Plus
(3.10 GHz, Intel Xeon Gold 6346)

SPECspeed®2017_int_base = 12.1
SPECspeed®2017_int_peak = 12.4

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Platform Notes (Continued)

CVE-2017-5753 (Spectre variant 1):
Mitigation: usercopy/swapgs barriers and __user pointer sanitization

CVE-2017-5715 (Spectre variant 2):
Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

CVE-2020-0543 (Special Register Buffer Data Sampling):
Not affected

CVE-2019-11135 (TSX Asynchronous Abort):
Not affected

run-level 3 Jun 22 16:42
SPEC is set to: /home/cpu2017_1.1.8

Filesystem   Type  Size  Used Avail Use% Mounted on
/dev/mapper/rhel-home xfs   670G  168G  502G  26% /home

From /sys/devices/virtual/dmi/id
Vendor:         HPE
Product:        ProLiant DL380 Gen10 Plus
Product Family: ProLiant
Serial:         CN70490X8B

Additional information from dmidecode 3.2 follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
32x Micron 36ASF8G72PZ-3G2B2 64 GB 2 rank 3200

BIOS:
BIOS Vendor:    HPE
BIOS Version:   U46
BIOS Date:      05/16/2021
BIOS Revision:  1.42
Firmware Revision: 2.40

(End of data from sysinfo program)

Compiler Version Notes

================================================================================
C       | 600.perlbench_s(peak)
================================================================================
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
  64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

(Continued on next page)
# SPEC CPU®2017 Integer Speed Result

**Hewlett Packard Enterprise**  
*Test Sponsor: HPE*

**ProLiant DL380 Gen10 Plus**  
*(3.10 GHz, Intel Xeon Gold 6346)*

**SPECspeed®2017_int_base** = 12.1  
**SPECspeed®2017_int_peak** = 12.4

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<th>CPU2017 License: 3</th>
<th>Test Date: May-2021</th>
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<td>Test Sponsor: HPE</td>
<td>Hardware Availability: Jun-2021</td>
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<td>Tested by: HPE</td>
<td>Software Availability: Jun-2021</td>
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## Compiler Version Notes (Continued)

```
C       | 600.perlbench_s(base) 602.gcc_s(base, peak) 605.mcf_s(base, peak)
| 625.x264_s(base, peak) 657.xz_s(base, peak)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
```

```
C       | 600.perlbench_s(peak)
```

```
C++     | 620.omnetpp_s(base, peak) 623.xalancbmk_s(base, peak)
| 631.deepsjeng_s(base, peak) 641.leela_s(base, peak)

Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,  
Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
```

```
Fortran | 648.exchange2_s(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on  
Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
```
SPEC CPU®2017 Integer Speed Result

Hewlett Packard Enterprise
(Test Sponsor: HPE)
ProLiant DL380 Gen10 Plus
(3.10 GHz, Intel Xeon Gold 6346)

SPECspeed®2017_int_base = 12.1
SPECspeed®2017_int_peak = 12.4

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE
Test Date: May-2021
Hardware Availability: Jun-2021
Software Availability: Jun-2021

Base Compiler Invocation

C benchmarks:
icx

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Base Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-DSPEC_OPENMP -std=c11 -m64 -fiopenmp -Wl,-z,muldefs -xCORE-AVX512
-O3 -ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

C++ benchmarks:
-DSPEC_OPENMP -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/opt/intel/oneapi/compiler/2021.1.1/linux/compiler/lib/intel64_lin/
-lqkmalloc

Fortran benchmarks:
-m64 -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto
-mbranches-within-32B-boundaries
Hewlett Packard Enterprise
(Test Sponsor: HPE)
ProLiant DL380 Gen10 Plus
(3.10 GHz, Intel Xeon Gold 6346)

SPECspeak®2017_int_base = 12.1
SPECspeak®2017_int_peak = 12.4

CPU2017 License: 3
Test Sponsor: HPE
Test Date: May-2021
Tested by: HPE
Hardware Availability: Jun-2021
Software Availability: Jun-2021

Peak Compiler Invocation

C benchmarks (except as noted below):
icx

600.perlbench_s: icc

C++ benchmarks:
icpx

Fortran benchmarks:
ifort

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:

600.perlbench_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)
-xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-strict-overflow
-mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

602 gcc_s: -m64 -std=c11 -Wl,-z,muldefs -fprofile-generate(pass 1)
-fprofile-use=default.profdumpdata(pass 2) -xCORE-AVX512 -flto
-Ofast(pass 1) -O3 -ffast-math -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

605.mcf_s: basepeak = yes

625.x264_s: -DSPEC_OPENMP -fiopenmp -std=c11 -m64 -Wl,-z,muldefs
-xCORE-AVX512 -flto -O3 -ffast-math
-qopt-mem-layout-trans=4 -fno-alias
-mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

657.xz_s: basepeak = yes
Hewlett Packard Enterprise
(Test Sponsor: HPE)
ProLiant DL380 Gen10 Plus
(3.10 GHz, Intel Xeon Gold 6346)

SPECspeed®2017_int_base = 12.1
SPECspeed®2017_int_peak = 12.4

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Test Date: May-2021
Hardware Availability: Jun-2021
Software Availability: Jun-2021

Peak Optimization Flags (Continued)

C++ benchmarks:

620.omnetpp_s: basepeak = yes
623.xalancbmk_s: basepeak = yes
631.deepsjeng_s: basepeak = yes
641.leela_s: basepeak = yes

Fortran benchmarks:

648.exchange2_s: basepeak = yes

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.0-ICX-revC.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.0-ICX-revC.xml